



VON ARDENNE Addresses Semiconductor Panel-Level Packaging Market with New HiPIMS Deposition Solution

HiPIMS deposition enables dense, highly adherent films for panel-level packaging applications

DRESDEN, Germany, Oct. 13, 2026 – [VON ARDENNE](#), a global leader in high-precision vacuum coating equipment and co-developed materials solutions, today announced that it is expanding its [semiconductor deposition portfolio](#) into panel-level [packaging](#) (PLP).

The HiPIMS solution deposits high-aspect-ratio barrier and seed layers in through-glass via (TGV) holes, enabling dense, highly adherent functional film deposition with improved material performance. It leverages the company's [HISS modular horizontal coating platform](#), which is designed for large-area deposition and provides the foundation for PLP process development and production. By applying HiPIMS technology to an industrial-scale production method on the HISS system, VON ARDENNE is scaling HiPIMS from wafer level processing to panel-level production.

“HiPIMS can reduce downstream costs,” said Dr. Holger Pröhl, head of technology and application at VON ARDENNE. “Better adhesion and denser films mean less rework, longer service life and, in some cases, eliminated process steps. For semiconductor manufacturers, HiPIMS can enhance yield and enable them to enter new product segments that demand higher-performance surfaces.”

HiPIMS with HISS technology allows semiconductor manufacturers to migrate established deposition processes from 300mm wafer formats to larger panel form factors for advanced packaging applications, including TGVs and redistribution layers (RDL). By enabling panel-scale deposition, VON ARDENNE helps customers improve manufacturing efficiency and accelerate PLP adoption.

Enabling the High-Growth Panel-Level Packaging Market

According to Yole Group, PLP generated more than \$300M in revenue in 2025 and is projected to grow by more than 40% CAGR over the next five years. PLP is set for strong acceleration toward 2029-2030, driven by TSMC's entry and the adoption of high-end PLP for AI and high-performance computing (HPC) applications, according to a [March 2026 Yole Report](#) titled “Panel Level Packaging 2026.”

“Panel-level packaging represents an important evolution in semiconductor manufacturing as well as a high-growth market, and deposition technology and reliable substrate handling is a critical enabler,” said Guido Ueberreiter, VP semiconductor strategy at VON ARDENNE.



“Our approach combines a scalable equipment platform with advanced deposition processes, allowing customers to transfer proven technologies to larger substrates while addressing the demanding uniformity and film-performance requirements of advanced packaging.”

Visit VON ARDENNE at SEMICON West 2026

For more information, visit <https://vonardenne.us/> or stop by the VON ARDENNE Booth 5373 at SEMICON West 2026, taking place October 13-15 in San Francisco’s Moscone Center.

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About VON ARDENNE

VON ARDENNE combines high-precision engineering and exceptional depth in materials science expertise to deliver advanced deposition and vacuum system solutions with configure-to-order flexibility and sub-nanometer precision for all substrate sizes and materials. With deep scientific expertise, flexible tool platforms and a collaborative approach, VON ARDENNE empowers semiconductor customers to scale from R&D to high-volume manufacturing and solve advanced coating challenges that conventional vendors can’t touch.

<https://www.yolegroup.com/product/report/panel-level-packaging-2026/>

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