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AI Meets Advanced Packaging: APhi Summit Puts the Spotlight on Heterogeneous Integration

As artificial intelligence continues to reshape semiconductor roadmaps, advanced packaging has moved from a supporting role to a primary driver of system performance. Few programs illustrate that shift more clearly than the Advanced Packaging & Heterogeneous Integration (APhi) Summit at SEMICON West 2026, where industry leaders will examine the technologies increasingly defining next-generation AI systems. Running October 13-15 at San Francisco's Moscone Center, the three-day program brings together experts from across the semiconductor ecosystem to address the challenges of integrating compute, memory, photonics, materials, and manufacturing into increasingly complex AI platforms.

The APhi agenda arrives at a pivotal moment for the industry. For decades, semiconductor performance gains were largely driven by transistor scaling. Today, AI workloads are exposing new bottlenecks in power delivery, thermal management, memory bandwidth, data movement, and manufacturing complexity. Across the APhi program, a common theme emerges: packaging is no longer simply enabling advanced semiconductor devices. Increasingly, it is becoming the architecture that allows disparate technologies to function as a coherent system.

Thermal Is the New Node

The summit opens on Tuesday, October 13, with the session "Thermal is the New Node: Managing Power in 3D Systems," highlighting one of the most pressing issues facing advanced AI hardware. As package complexity and power density continue to increase, thermal performance has become a primary determinant of system capability, reliability, and scalability. The opening keynote, "The Architecture of Intelligence: Advanced Packaging for AI at Scale," will be delivered by Ingu Yin Chang, Executive Vice President of ASE. His presentation explores how advanced packaging is evolving to support increasingly complex AI systems and examines challenges spanning bandwidth, power delivery, energy efficiency, heterogeneous integration, and

manufacturing scalability. As AI expands beyond cloud computing into robotics, physical AI, and intelligent edge systems, the ability to integrate diverse technologies efficiently may become as important as advances in silicon itself. Additional presentations address thermal characterization, power delivery, thermal process control, and virtual manufacturing approaches for advanced packaging and HBM integration. The session underscores how power and thermal considerations are increasingly shaping advanced packaging roadmaps.

The Gatekeepers of Yield

Tuesday afternoon shifts the focus from performance to manufacturability with "The Gatekeepers of Yield in Advanced Packaging," a session devoted to metrology and inspection technologies that are becoming critical as heterogeneous integration moves toward high-volume production. One of the strongest messages emerging from the session is the growing convergence between front-end and back-end semiconductor manufacturing. Processes such as hybrid bonding, TSV formation, wafer-to-wafer alignment, and chiplet integration increasingly require the type of precision and process control once associated exclusively with leading-edge wafer fabrication. As interconnect pitches shrink and package architectures become more complex, maintaining yield becomes an increasingly sophisticated challenge. Presentations from Intel, EV Group, QuantumDiamonds, and EMD Electronics will explore advanced metrology strategies, non-destructive inspection techniques, optical process control, and yield-learning strategies for complex package architectures. The session highlights a reality confronting much of the industry: scaling heterogeneous integration is as dependent on process control as it is on architecture innovation.

Co-Packaged Optics Takes the Stage

The conversation then turns to data movement during Tuesday's session, "Co-Packaged Optics (CPO): Powering the Next Wave of AI Connectivity." As AI systems continue to scale, moving data efficiently has become one of the industry's most significant technical challenges. The session brings together perspectives from NVIDIA, UConn, Tescan, Lam Research, and AIM Photonics. Topics range from AI-enabled ultrafast-laser manufacturing for photonic packaging and equipment strategies for heterogeneous integration to end-to-end approaches for photonic integrated circuits and advanced optical packaging. Several presentations focus on the manufacturing infrastructure needed to support optical integration at package level. Others address photonic interposers, optical alignment technologies, and the packaging challenges associated with integrating photonic and electronic devices. Collectively, the session reflects the expanding role of photonics within the heterogeneous integration ecosystem and its potential contribution to future AI infrastructure.

Breaking the Integration Wall

Wednesday opens with "Equipment Frontiers for Advanced Packaging - From Hybrid Bonding to Co-Packaged Optics," a session focused on the manufacturing technologies needed to support future AI architectures. The featured presentation, "Breaking the Integration Wall: Advanced

Packaging for the AI Era," from Lam Research, examines how AI workloads are pushing current packaging technologies toward their practical limits. Topics include high-density TSVs, hybrid bonding, chiplet reintegration, photonics-memory-compute co-packaging, and the manufacturing innovations needed to support increasingly heterogeneous architectures.

Materials Innovation Enables the Full Stack

Packaging innovation is not limited to equipment and process technology. Wednesday's session, "Materials Innovation for Heterogeneous Integration: Enabling the Full Stack," examines the materials foundation supporting next-generation semiconductor systems. Presentations from Michael Joerger of Heraeus and Takenori Fujiwara of Toray highlight the breadth of materials innovation supporting heterogeneous integration. Joerger will discuss developments in solder materials, thermal interface materials, sintered die attach technologies, and technical ceramics such as aluminum nitride and alumina, while Fujiwara will focus on advanced polymer, dielectric, temporary bonding, and optical packaging materials for AI, HPC, and photonic integration applications.

Federal Programs and Strategic Investment

Beyond technical innovation, the APhi Summit also examines the broader ecosystem supporting advanced packaging development through discussions of research infrastructure, workforce development, and government-supported initiatives. Wednesday afternoon highlights DARPA's Next Generation Microelectronics Manufacturing (NGMM) program—establishing the nation's first pure-play 3DHI center at UT Austin/TIE—alongside CHIPS R&D Office (CRDO) projects such as Multibeam's maskless e-beam lithography for fine-pitch interconnects. Presenters will also address critical hardware security in 3D ICs and workforce training programs required to scale domestic packaging ecosystems.

Looking Beyond Today's Packaging Paradigm

The APhi Summit concludes on Thursday with the IEEE IRDS Session on Packaging Integration (PI), which takes a longer-term view of where the industry may be headed. Topics are expected to include emerging 2D, 2.5D, 3D, and wafer-scale integration approaches, along with novel substrate technologies and future packaging architectures designed to sustain AI growth. By the time APhi concludes, attendees will have examined topics spanning thermals, metrology, hybrid bonding, photonics, advanced materials, manufacturing ecosystems, federal research initiatives, and long-term technology roadmaps. The breadth of the program reflects an important reality facing the semiconductor industry: artificial intelligence is transforming advanced packaging into a foundational system-level discipline.