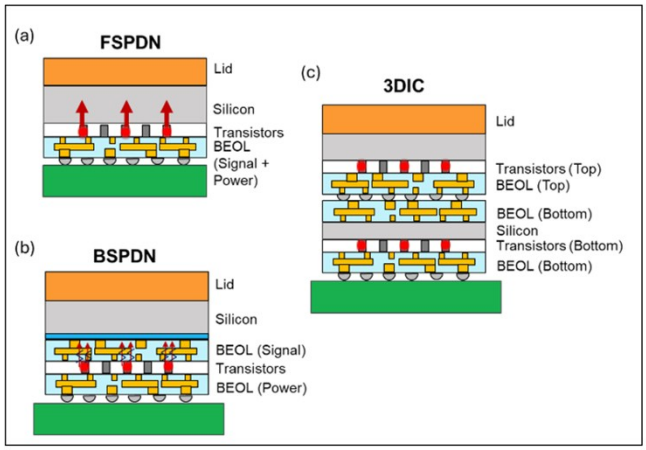
Reliability Technologies to be Featured at 2025 Electronic Components & Technology Conference

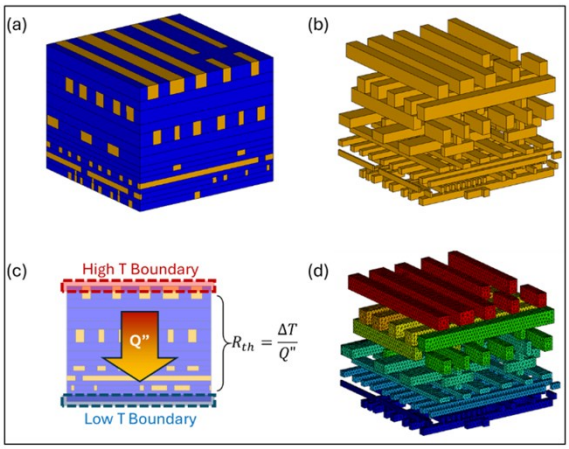
Machine Learning for Better Thermal Management

Thermal management is one of the most critical issues impacting the performance and reliability of next-generation electronics packaging technologies. That's because new architectural features such as backside power delivery networks (BSPDNs) and 3D IC configurations introduce new components within the thermal pathway, creating additional heat dissipation challenges. To optimize thermal management, better estimation of chip and package temperatures is required. But while analytical approaches to estimate BEOL interconnect-layer thermal resistance have been developed, they are inadequate.

At ECTC, IBM researchers will describe how they used a series of finite element modeling (FEM) simulations to train a machine learning (ML) model to rapidly predict the thermal resistance of BEOL stacks in a test chip. BEOL layout design, heights and material information were used as inputs. The researchers say the ML model predicted the thermal resistance of BEOL stacks with a mean absolute percentage error (MAPE) of less than 15%. That is a remarkable accuracy improvement versus the traditional 1-D heat conduction analytical model used for comparison, which showed a MAPE of 300%. The machine learning approach opens the possibility of more accurate predictions of hotspots in advanced packaging architectures, thus helping to increase their performance and reliability.

IP session #37, "*Fast And Accurate Machine Learning Prediction of Back-End-Of-Line Thermal Resistances in Backside Power Delivery and Chiplet Architectures*," P. Chowdhury et al, IBM



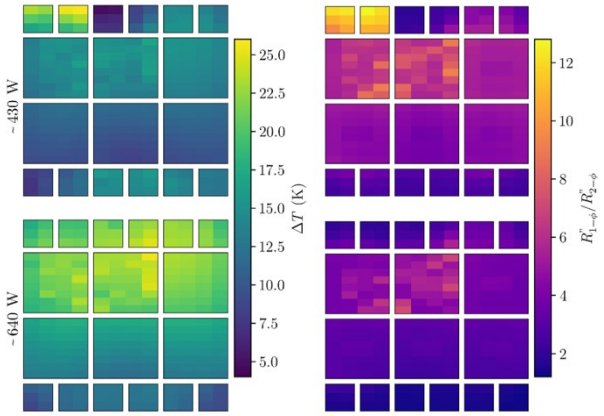


- **At left above** are a series of schematics showing increasingly complex thermal pathways in (a) a 2D front-side power delivery network (FSPDN) package; (b) a 2D BSPDN; and (c) a 3D IC package with two dies.
- **At right above** is a representative 3D BEOL sub-stack model with (a) dielectrics included and (b) dielectrics removed for visualization. (c) is a schematic of the finite element model setup for thermal resistance extraction, and (d) is a representative temperature profile in the metal.

A Tool for Optimized Cooling of High-Performance Systems

Cooling the high-performance computing systems in AI datacenters, 5G radio access networks (RAN), and edge compute nodes is a growing challenge. That's because the multi-chip modules (MCMs) used in these systems, which integrate CPUs, GPUs, and high-bandwidth memory (HBM) in 2.5D/3D architectures, already draw more than 1000 watts, and that will increase going forward.

A Nokia Bell Labs team will describe a high-power thermal test vehicle (TTV) they built to assess the efficiency of various novel cooling solutions. At its core is a multi-chip module (MCM) consisting of six emulated logic dies and 12 emulated HBM stacks. These are mounted on a ceramic interposer capable of dissipating more than 2600 W, with localized hotspots reaching 314 W/cm² (and 817 W/cm^2 over the heater resistor area). The MCM has 264 platinum-based resistive temperature detectors for high-resolution thermal monitoring. It enables independent power control across 60 heater regions, facilitating the creation of diverse heat maps of discretized regions across the MCM surface. This capability enables the study and optimization of various novel cooling technologies. In addition, the TTV was integrated into a pumped two-phase refrigerant cooling system, which successfully handled heat fluxes up to 314 W/cm² over a 46 mm^2 hotspot on each logic die. By reducing peak chip temperatures as much as 25°C, it highlights the superior thermal performance of two-phase versus single-phase cooling.
IP session #40, "*Experimental Demonstration of High-Power Thermal Test Vehicle using Two-Phase Cooling for AI Datacenters, 5G RAN, and Edge Compute Nodes*," Yang Liu et al, Nokia Bell Labs



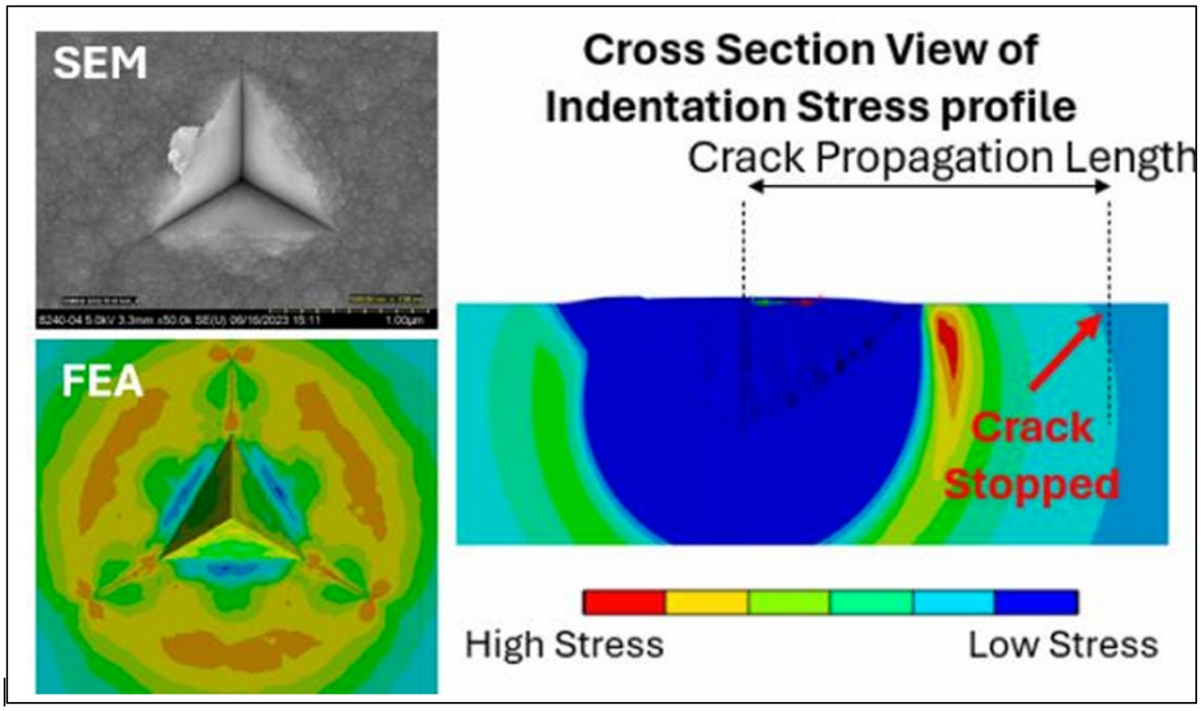
- **<u>At left</u>** is a photo of the fabricated single-substrate multi-chip module (MCM) with 18 thermal test chips. The six larger chips are the logic dies, while the 12 peripheral chips are high-bandwidth memories.
- **<u>At right</u>** are thermal maps comparing the performance of single- and two-phase flows, represented by the difference in the MCM temperatures (left column) and the ratio of the specific thermal resistances (right column) of single- and two-phase tests conducted at ~ 430 W and ~ 640 W (top and bottom rows, respectively).

Better Predictions of Thin-Films' Plasticity and Fracture Behavior

Brittle thin films such as silicon dioxide, silicon nitride and others are widely used in semiconductor devices, where their mechanical reliability is critical. It's difficult to accurately characterize the plasticity and fracture properties of thin films at sub-micron scales, though, because of the limitations of conventional mechanical testing methods. Yet understanding these properties is essential because they directly influence film deformation and crack behavior during the manufacturing process. These, in turn, affect the performance and reliability of the microelectronics and memory devices made from these films.

At ECTC, a University of Singapore/Micron Technology team will describe a novel methodology for predicting thin-film plasticity and fracture properties by integrating finite-element analyses (FEA) simulations with experimental nanoindentation data. (Nanoindentation is where a controlled force is applied to a material's surface using a sharp indenter, and the resulting deformation is then analyzed.) The experimental results show a strong correlation between the simulations and the observed fracture behavior, validating the methodology. The researchers say this framework offers a more cohesive, easier-to-implement alternative to traditional modeling methods, and it can be extended to also predict the behavior of ductile thin films; the adhesion strength between layers; and the porosity of low-k dielectric materials, broadening is applicability.

Paper 24.5, "*Predictive Modelling of Thin Films Properties Using An Experimental and Simulation-Based Approach*," D.K. Lim et al, Nat'l Univ. of Singapore/Micron Technology



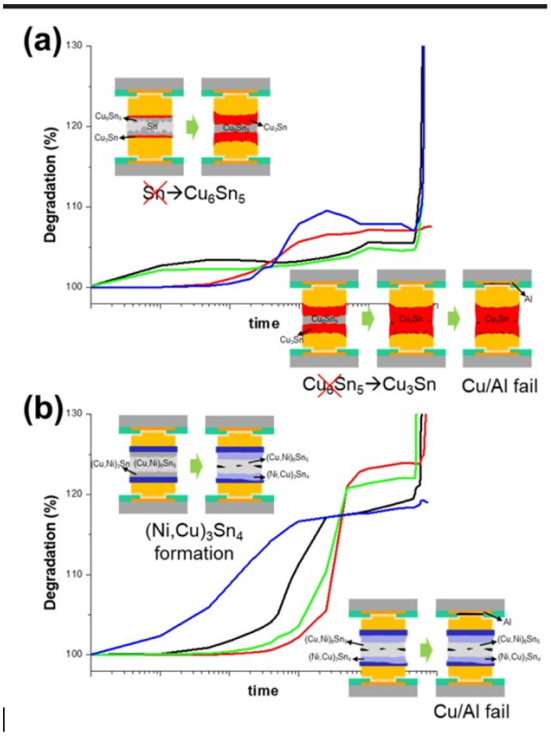
- **The image above** compares (on the left side) an SEM view of a deliberately induced crack in an SiO_2 thin film with the FEA prediction of what it would look like, showing excellent agreement. The right side of the image is an analysis of the calculated "stress intensity factor," which corresponds to the actual crack propagation length.

Microbumps and Electromigration

As the electronics industry pushes the boundaries of miniaturization to the angstrom level, reliability is a growing concern. One area of focus is the solder microbump, used to interconnect chips within multichip modules, and to connect chip packages to printed circuit boards (PCBs). As microbumps shrink and the current density flowing through them increases, a phenomenon called electromigration (EM) is more likely to damage them. EM is where the flow of electric current actually causes the conductor material to move, creating voids or short circuits within it. A better understanding is needed of how EM occurs in materials commonly used to make ultrasmall microbumps, and how it can be prevented.

At ECTC, TSMC researchers will describe studies they conducted to do that. They investigated the EM performance of microbumps made from Cu/Sn and Cu/Ni/Sn/Cu in a full, complete intermetallic compound (IMC) structure. IMC is the interface layer where the solder and the base metal meet. It is formed during the soldering process. The researchers will report that full IMC microbumps are robust enough to withstand EM. Further, when EM does occur its main failure mode is failure of the aluminum (Al) traces, caused by the electromigration of Al atoms. This finding underscores the importance of forming full IMC joints to enhance the reliability of microbumps in demanding applications such as high-performance computing.

Paper 28.4, *"The Influence of Full IMC Structure on Micro-Bump Electromigration Performan_ce,"* Chung-Yu Chiu et al, TSMC

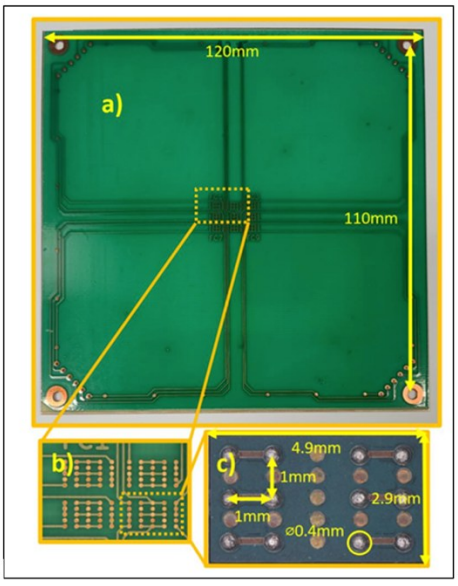


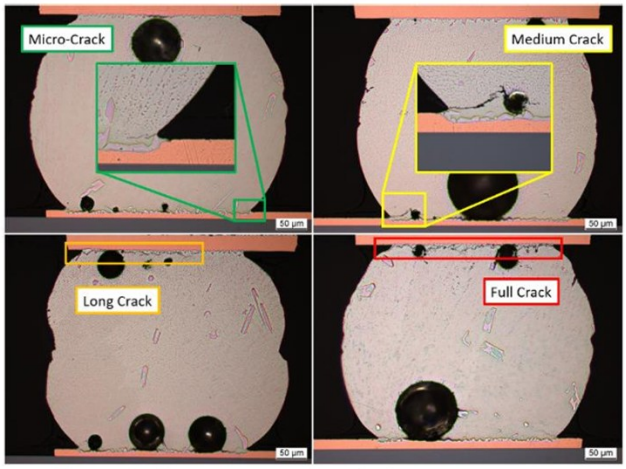
- **<u>The image above</u>** is a schematic diagram showing how the microstructures of (a) Cu/Sn and (b) Cu/Ni/Cu/Sn <u>non-full IMC</u> microbumps changed during electromigration testing, culminating in the failure of aluminum traces.

Shock Testing Flip-Chip Interconnects

Increasingly sophisticated electronic systems are being more widely deployed in harsh, real-world applications such as automotive, avionics, industrial production and others. That means thermal/mechanical issues like heat, vibration and shock are more critical because of their potential reliability impacts. But existing shock/vibration test methods and equipment are falling short because they were designed for less complex electronic systems. At ECTC, TU Dresden researchers will describe better ways to simulate and perform shock testing under real-world conditions. They will unveil a new test vehicle for shock and other mechanical loads, which can test multiple components simultaneously. In the initial design, their test board consisted of nine flip-chips (2.9 x 4.9mm²) mounted in a 3x3 matrix configuration. They were tested until failure under shock loads of 130g amplitude/2ms pulse width, and at -40°C, room temperature, and 125°C. Failure analysis after the tests showed crack initiation, propagation and even some complete cracks near the solder joints on both the flip-chip and board sides of the joints. The researchers say these results will serve as a basis for better shock profiles, measurement practices and fixture methods for future testing, and for testing with a mixture of loads as well.

Paper 18.7, "*Isothermal Shock Testing on Flip-Chip Interconnects*," M. Häusler et al, TU Dresden





The images above show:

- At left (a) is the newly developed test board; (b) is the flip-chip array; and (c) is the flip-chip test component.
- At right are cross-sectional photos of the various damage states seen in the solder joints.

For more information about the 2025 ECTC program, please visit:
https://www.ectc.net/PROGRAM/index.cfm