Revolutionizing IC Packaging with High-Density RDL Technology

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The demand for high-performance devices, particularly in AI, HPC, and data centers, has surged dramatically in the ever-evolving landscape of integrated circuit technology. This demand has been further accelerated by the COVID-19 pandemic, pushing the boundaries of silicon technology to its limits. Enter Amkor's S-SWIFT™, a packaging solution designed to address these challenges and revolutionize the IC packaging industry.

The need for advanced packaging solutions

As the industry strives to minimize silicon technology nodes, currently at the 3 nm mark, the associated costs and development times have skyrocketed. The smaller the node size, the higher the risk of defects, leading to lower wafer yields. Chiplet technology has emerged as a viable solution to these limitations, enabling the separation of core blocks into smaller dies, thereby improving wafer yield and reducing design costs. However, interconnecting these heterogeneous block dies requires advanced IC packaging technologies.

The evolution of IC packaging

Traditionally, multi-chip module (MCM) flip chip ball grid array (FCBGA) packaging has been used for heterogeneous interfaces of multi-chips on laminate substrates. However, this approach falls short for advanced node ICs due to the long electrical paths of the substrate. The introduction of 2.5D Through Silicon Via (TSV) technology offered a shorter electrical path but was limited by performance issues in high-frequency applications. This led to the development of high-density fan-out (HDFO) interfaces, which excluded silicon and inorganic dielectrics in favor of organic dielectrics.

S-SWIFT: A game-changer

Amkor Technology's S-SWIFT (Substrate Silicon Wafer Integrated Fan-out Technology) package stands out in the HDFO landscape. It provides higher bandwidth and die-to-die interconnects for heterogeneous integration with a high-density interposer. The S-SWIFT methodology addresses several critical design aspects, including fine pitch, µ-bump interfaces, accurate warpage control during thermal assembly, capillary under-fill, over-molding techniques and the mold-side bumping process.

One of the core technologies in S-SWIFT is the high-density redistribution layer (RDL) technique. In HDFO packaging, the RDL provides the chip-to-chip interface, and higher-density RDL is essential for interconnecting chips with smaller node-size blocks. The semi-additive process (SAP) has been the mainstream technology for RDL fabrication, but it faces challenges in defining fine pitch features. To overcome these issues, a dual damascene process with an organic dielectric has been proposed, embedding the RDL in the organic dielectric to prevent seed layer undercut issues.

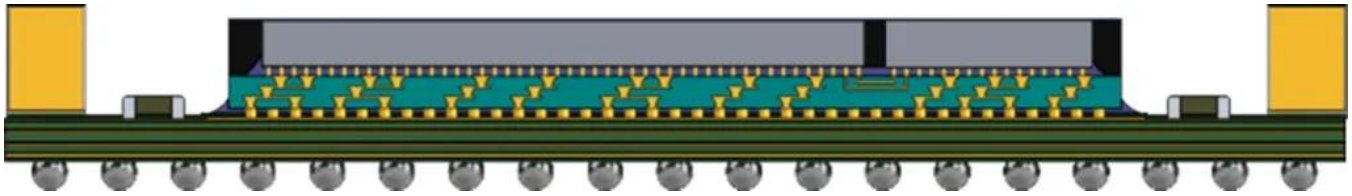

Fig. 1: S-SWIFT.

Embedded trace RDL (ETR) process

The embedded trace RDL (ETR) process is a significant advancement in RDL fabrication. It involves embedding the trace in the dielectric layer without an etch process, addressing challenges such as seed layer undercut, and sidewall etch issues. The dual damascene copper (Cu) structure in the ETR process offers advantages in high-frequency signal pass characteristics, as the smooth Cu surface is less affected by electron scattering.

ETR also simplifies the RDL fabrication process, reducing the number of steps by 40% compared to the current dual damascene method and 33% compared to SAP. This reduction in process steps translates to lower costs and improved efficiency. The ETR process has demonstrated excellent patterning capability, achieving trench patterns with 2/1-µm line/space dimensions and various via sizes.

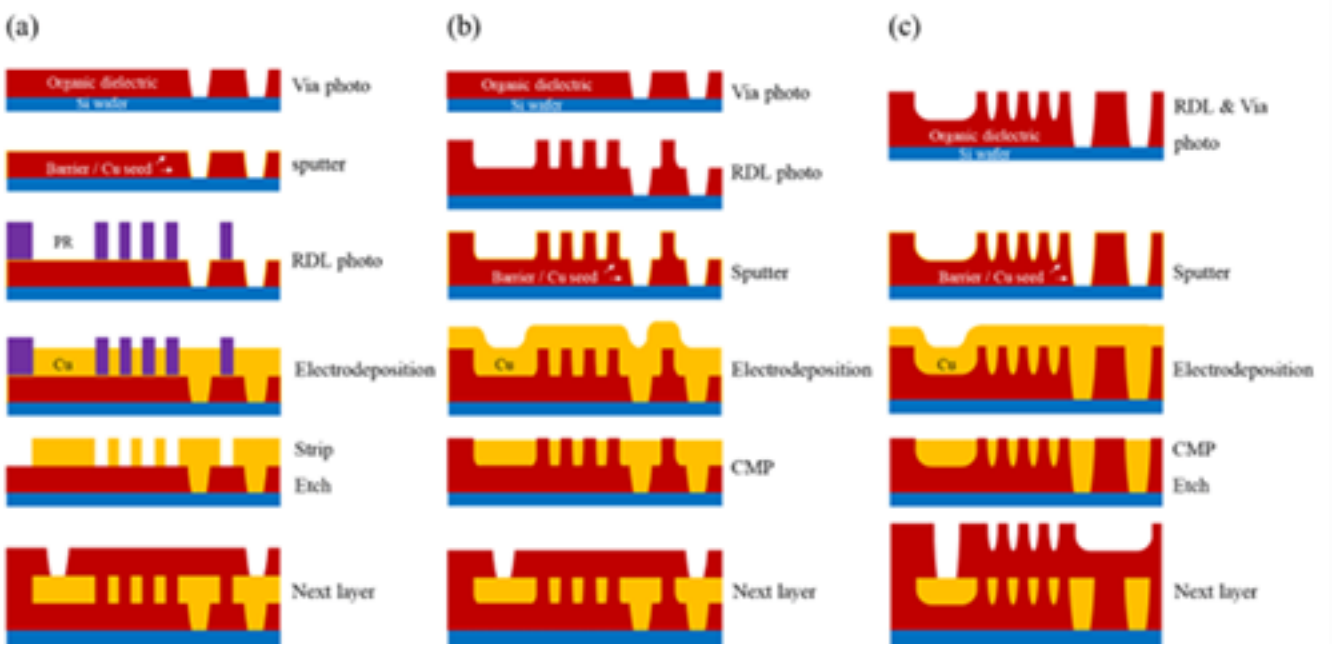

Fig. 2: Schematic diagrams of RDL process flow by (a) semi-additive process (SAP), (b) dual damascene process and (c) new embedded trace RDL process.

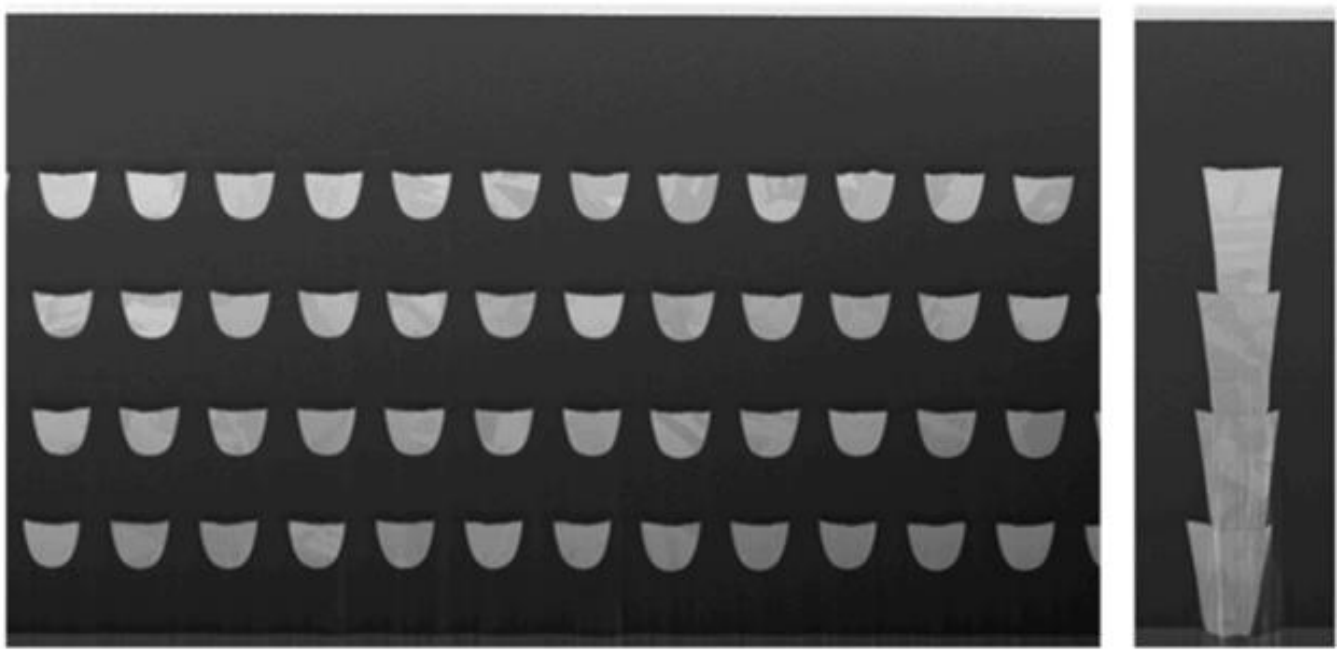

Fig. 3: Cross-sectional images of a 4-layer RDL with 2/1 µm of line width/space and a 2 µm stack via formed by the ETR process.

Reliability and performance

The reliability of the ETR structure in the S-SWIFT package has been thoroughly tested. The seed layer surrounding the three faces of the ETR acts as a barrier, preventing Cu ion migration and ensuring reliability under conditions of current, heat, and humidity. The S-SWIFT package with ETR has passed industry-standard reliability tests, including moisture soaking, temperature cycling, unbiased highly accelerated stress tests, and high-temperature storage tests.

Conclusion

Amkor Technology's S-SWIFT packaging with embedded trace RDL represents a significant leap forward in IC packaging technology. By addressing the limitations of traditional packaging methods and offering a reliable, high-performance solution, S-SWIFT is poised to meet the growing demands of AI, HPC and data center applications. As the industry continues to push the boundaries of silicon technology, innovations like S-SWIFT will play a crucial role in shaping the future of high-performance computing. To learn more, visit Amkor.com/s-swift

For more information about Amkor's S-SWIFT™ visit: **https://amkor.com/s-swift/**