Ensuring Large Die Durability in AI and HPC Advanced Packages

Protection is Performance-Critical, Processability is Production-Vital

Chunlin He, Tim Champagne, Arsia Khanfekr, Kail Shim, Raj Peddi, Ramachandran Trichur
Henkel Corporation

Nothing has illuminated the significance of advanced semiconductor packaging more than the data age and the recent, well-publicized growth of artificial intelligence (AI) and high-performance computing (HPC). Though advanced packaging designs have been in use for decades, significant progress in 2.5D and 3D heterogeneous integration has been made over the last ten years to dramatically increase I/O, improve performance, realize cost-efficiencies, reduce power, and accelerate signal speeds for massive data processing. Advanced packaging innovation is the primary enabler of powerful, high-bandwidth AI and HPC devices.

Complex Large Body, Large Die Packages

There is a diverse range of advanced packaging platforms, including fan-out wafer-level packaging/ 2.5-D, 3-D stacked packaging, and system-on-a-chip (SoC). Several AI and HPC technologies leverage high-density fan-out HD-FO (or ultra-high-density fan-out)/2.5-D and 3-D technologies, while other computing applications for servers, networking, gaming, and edge devices may use flip-chip BGA (FCBGA) designs. Next-generation HD-FO/2.5-D packages generally have sizeable footprints, integrating very large die. There are many examples of these designs -- such as CoWoS® and I-Cube®, to name a few -- developed by the world's top semiconductor companies. While approaches and architectures vary, these technologies typically integrate a large interposer die/redistribution layer (RDL) on which other die – logic, compute, and stacked high bandwidth memory – are integrated. The result is a sizeable package body, making processing and protection even more challenging. For example, the CoWoS (chip-on-wafer-on-substate) 2.5D platform, well-known in the AI and HPC GPU space, has seen several iterations. According to IEEE, the fifth generation of this technology may see CoWoS packages with interposers measuring 2500 mm2. This is but one of many new HD-FO/2.5-D advanced packaging designs tackling the demands of AI and HPC which, according to market analyst Prismark, is a category that will see nearly 35% CAGR over the next five years. With these new advanced packages, however, come challenges – particularly in relation to ensuring the reliability of large – *and getting larger* --, high-density I/O die. Protecting against thermal-mechanical stress and die warpage for die of this scale while complying with processing demands is imperative.

Die Protection is Vital to Package Reliability and Performance

Underfill materials, introduced in the late 1990s to fortify PCB direct chip attach, are now essential for advanced semiconductor packaging to improve interconnect reliability. The epoxy-based materials protect against thermal-mechanical stress induced by coefficient of thermal expansion (CTE) variances between substrates and die. This capability guards against factors like warpage and die cracking that can render an entire device inoperable. There are multiple package-level underfill formats (non-conductive paste, non-conductive film, and capillary), and their effectiveness depends primarily on interconnect pitch, gap height, and processing preference. However, capillary flow underfills are preferred when it comes to HD-FO/2.5-D devices with bump pitches less than 100 µm and gap heights below 50 µm.

The difficult – but critical – task of protecting large die (>20 mm x 20 mm) I/O cannot be underestimated, and ensuring complete, void-free bump encapsulation using capillary flow underfills is challenging given the required coverage surface area and dimensional complexity. The materials not only have to deliver the adhesion, cured rigidness, high toughness, and crack resistance required to secure die in-application, but must be formulated with a rheology that enables fast flow, high UPH, and total die I/O coverage before material gelation occurs.

Capillary Underfill Innovation Overcomes Dimensional Challenges

An underfill development project to tackle the dimensional and processability obstacles associated with large die integration in AI and HPC devices was recently completed. A balanced formulation that meets the flow characteristics, low warpage, crack resistance, toughness, and long-term reliability performance required for large die, flip chip BGA and Cu-pillar, highly integrated advanced semiconductor packages resulted in the development of Loctite Eccobond UF 9000AE. The material meets demanding metrics to enable current and next-generation large die advanced packages.

Rheology Designed for the Unique Characteristics of Large, High-Density I/O Die

Rheology optimization is one of the most challenging formulation aspects for large die capillary underfills. Rheological properties that enable the material to flow quickly within miniaturized interconnect pitch and gap dimensions for clean underfilling across a large surface area while providing high filler loading for maximum protection are essential. If the material flows too slowly, it may not only limit UPH, but can begin to gel before complete die interconnect coverage is achieved, adversely affecting reliability. The new capillary underfill is a highly-filled material (~70% filler loading) that offers faster underfilling for more efficient edge-to-edge die coverage. In testing on die as large as 40 mm x 40 mm with >2,000 100 µm pitch bumps with 50 µm gap heights, Loctite Eccobond UF 9000AE demonstrated up to 20% faster flow* versus previous-generation materials. (**Figure 1**) The material has been verified on die as large as 50 mm x 50 mm and its flow characteristics indicate compatibility with even larger die, supporting the evolution of HD-FO/2.5-D packaging. Importantly, this material's resin system limits resin bleed out (RBO) to enable the tight keep-out-zones necessary for highly integrated advanced packages.

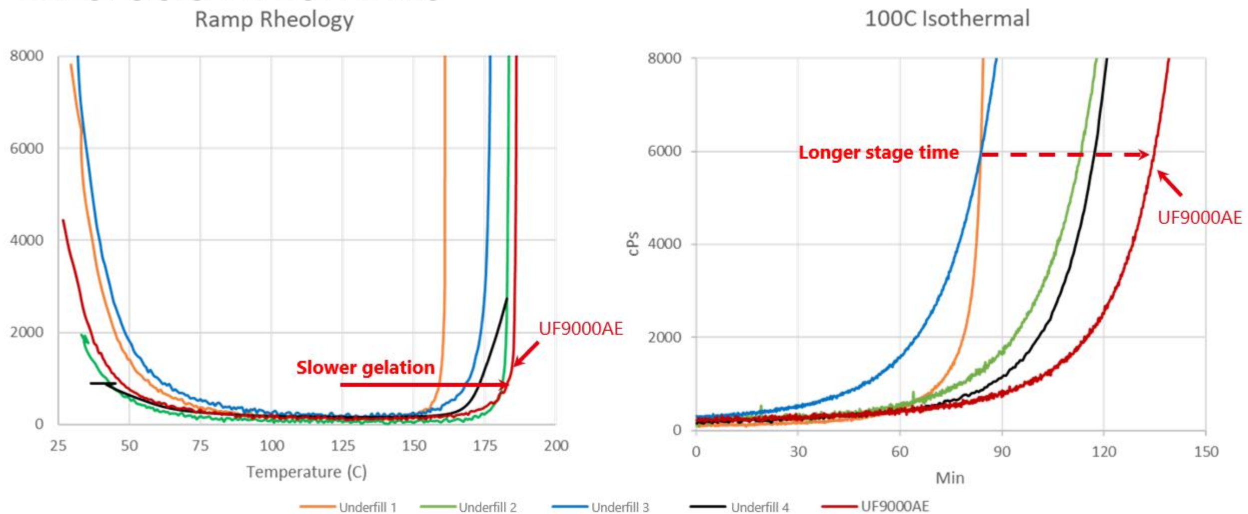

Figure 1: As compared to previous-generation materials, Loctite Eccobond UF 9000AE's rheological properties provide a longer stage time (up to 100 minutes) and slower gelation to enable complete bump encapsulation.

Low Stress, Low Warpage, and High Crack Resistance

The most common failure mode within large die applications is die cracking, so formulating a material with properties optimized to prevent crack-related failures is critical for large die capillary underfills. With a low coefficient of thermal expansion (CTE) (23 ppm/℃ below Tg), low modulus (13.5 GPa at 25℃), and a high K1c (3.0) (**Figure 2**), Loctite Eccobond UF 9000AE's material properties are well-balanced to address the challenges with die sizes measuring >20 mm x 20 mm and as large as 50 mm x 50 mm*. The formulation offers a low-stress, lower warpage solution for large die, significantly reducing the propensity for interconnect damage due to stressors like temperature differentials and warpage.

LOCTITE® ECCOBOND UF 9000AE

TOUGHNESS (K1C) / CRACK RESISTANCE

Fracture Toughness (K1c) and CTE improvement

Properties	Unit	Underfill 1	Underfill 2	UF 9000AE
Filler Loading	%	60	50	68
Toughness (K1c)	MPa√m	2.0	0.6	3.0
CTE1/CTE2	ppm/°C	25/100	30/119	23/84
Shrinkage	%	1.8	2.2	1.1

Figure 2: In testing versus other underfills, Loctite Eccobond UF 9000AE showed higher fracture toughness and lower CTE and shrinkage, resulting in low stress on large die packages.

Safety and Sustainability

While material characteristics and reliability performance are foremost, compliance with industry regulatory standards and the assurance of operator safety have also been considered in the development of Loctite Eccobond UF 9000AE. The material contains no SVHCs per REACH regulatory standards and is also PFAS-free.

A Milestone for Advanced Packaging

Introduced in 2000 – nearly a quarter of a century ago! – advanced packaging's ability to aggregate devices has witnessed, some would argue, its most significant progress in the last decade. Without

the sophistication of highly integrated packaging alongside the continued evolution of advanced Si node chips, much of today's semiconductor capability – particularly for the powerful computing sector – would not be possible. Thorough interconnect protection is vital to the assurance of its continued development.

Learn more by joining us for this webinar.

Talk to a technology specialist.

**Die size dependent*.