TSV RESIST AND ETCH RESIDUE REMOVAL FOR 3DIC

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ABSTRACT

The main driving force for technology advancement for consumer electronics in the semiconductor industry over the last few years has been increased functionality in a small footprint. 3D integration is the most promising methodology for providing that increase in device performance and density. This methodology has forced the development of processes for manufacturing stacked and vertically interconnected chips, connected by silicon or glass interposers, or directly using through silicon vias (TSVs). There are numerous technical papers and presentations on the etching and filling of these vias, however the process for cleaning is seldom mentioned. TSVs are formed using a two-step process called deep reactive ion etching (DRIE) or the Bosch process, that alternately etches and then passivates the Si side wall of the etch feature. The use of fluorinated gases in the passivation step allows for the formation of fluorinated organic molecules, which protect the silicon surface and allow the etch process to proceed in a more directional manner. However, the fluorinated passivation layer remains on the surface at the end of the process and must be removed subsequently.

Industry accepted formulations for removal of polymers and post etch residue after RIE processes typically are water-borne solutions. Removing the fluorinated residues produced during DRIE has required a shift from the aqueous formulations used in conventional residue removers to solvent-borne formulations. These formulations must be optimized to remove the

fluorinated passivation and any polymeric residue in addition to providing enhanced compatibility necessary for high performance devices.

This paper describes a robust cleaning process for one step removal of both the photoresist and sidewall polymer residues from TSVs in an immersion process. SEM, EDX and Auger analysis illustrates the cleanliness levels achievable with the reported process.
Keywords: Cleans, TSVs, non-TMAH, Bosch process, etch residue

INTRODUCTION

Three dimensional integrated circuit (3DIC) integration is defined as stacking an array of two dimensional (2D) chips to create the third dimension, using TSVs, thinned chips or interposers, and micro solder bumps (μ-bumps) to form connections and achieve improved performance and small form factor. Two groups of 3DIC integration schemes exist, direct chip stacking and stacking with active or passive interposers sandwiched in between chips, as shown in Figure 1.

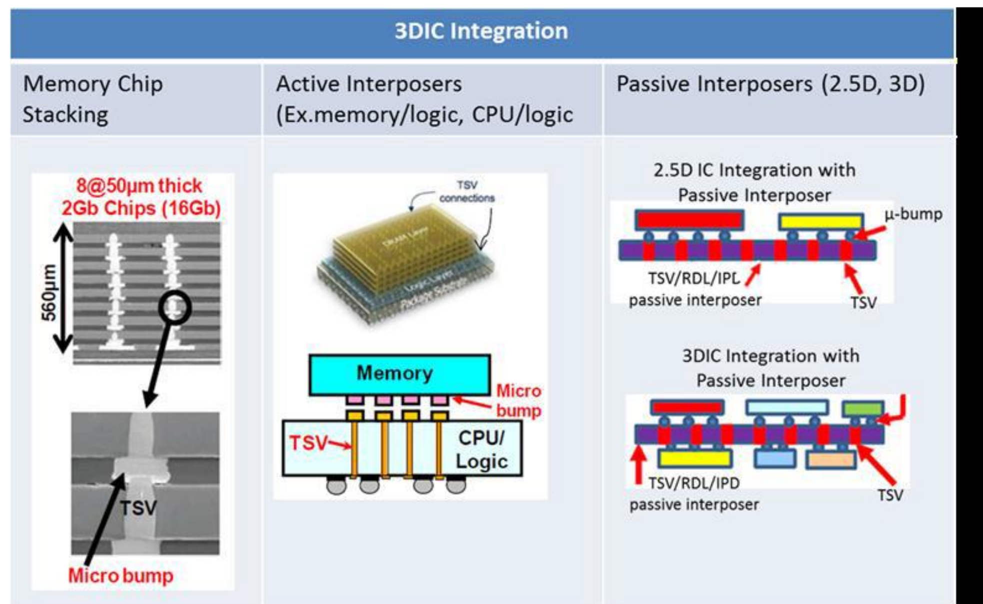

Figure 1. 3DIC integration schemes

The industry has been working towards defining standards and developing infrastructure to move 3DIC manufacturing schemes into high volume manufacturing. Passive interposers with TSVs are the most direct path to realization. Two kinds of passive interposers have been developed, one uses 2.5DIC integration and the other uses 3DIC integration. Figure 2 shows a

typical system-in-package (SiP) test vehicle for 3DIC integration. This vehicle was used by ITRI.1

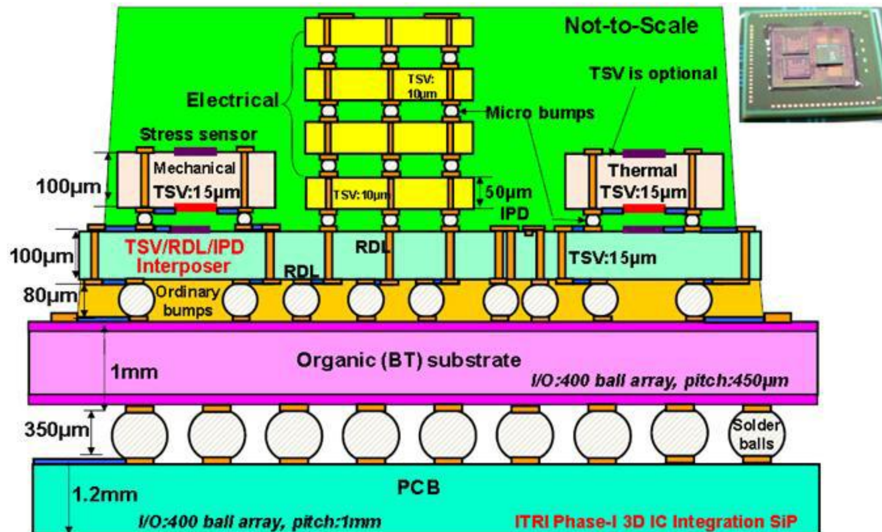

Figure 2. ITRI's Phase-I 3D IC integration SiP test vehicle.1

Most TSVs are formed using deep reactive ion etch (DRIE). The etch rate is the most important factor for obtaining high-quality TSVs with smooth vertical sidewalls with minimal scalloping. However, minimum scalloping and smooth vertical sidewalls are optimized with increasing process time. Efforts are made to balance out the two variables to provide acceptable vias with sufficient throughput. Typically, sulfur hexafluoride (SF6) will be used in etch cycle, while octafluoropropane (C3F8) will be used in passivation cycle. The use of C3F8 to create the passivation layer results in a residue that is highly fluorinated and thus very difficult to remove. Additionally, since the process does not also include use of oxygen or other strongly oxidizing species, the residue is chemically very different than those formed in the more traditional RIE process (which often uses tetrafluoromethane, CF4 and oxygen O2). DRIE has been used in MEMS manufacture for many years. However, introducing it into packaging-related schemes with unique cleaning and compatibility challenges has created an opportunity for new solutions to be developed. Removing DRIE residue has typically been accomplished using a dry plasma-based ashing process, often followed by a formulated cleaning solution to remove any remaining oxidized residue. However, removing the fluorinated residues produced during DRIE without an intervening ashing step has required a shift from conventional aqueous formulations to solvent-borne formulations. These formulations must be optimized to remove the fluorinated passivation layer and any polymeric residue in addition to providing enhanced compatibility necessary for high performance devices.

Solvent-based cleaning solutions, such as Dynastrip™ AP7880-C and CoatsClean™ ER105, both of which contain tetramethylammonium hydroxide (TMAH) have been reported on previously,2

and have been used successfully in large volume manufacturing for this purpose. They are highly effective in challenging processes such as removing etch residue after TSV formation. However, with each cleaning process there are both benefits and drawbacks. For TMAH-based products, the benefits are good cleaning, excellent compatibility, moderate process and temperatures, with good integration into existing device processes and fabs. However, the characteristics that can provide challenges include a shorter bath life when operated above room temperature and more recently, an increased concern about toxicity, that requires more extensive EH&S oversight.3 In a continued effort to improve the health and safety of photoresist and residue removal products, there is great demand to provide an effective non-TMAH containing solution for residue removal.

This paper describes a robust cleaning solution for one step removal of both the photoresist and sidewall polymer residues from TSVs in an immersion process. The solution capabilities are compared between a new non-TMAH containing post-Bosch process cleans formulation and two commercially known post-Bosch process etch residue removal products. SEM, EDX and Auger analysis illustrates the cleanliness levels achieved.

EXPERIMENTAL

Silicon wafers patterned with TSVs, (diameter 10μm, depth 100μm, minimum pitch 18μm) using a DRIE process were cleaved into ~2.5 x 4 cm2 coupons. Enough coupons were cleaved to investigate the following conditions: (a) coupon with no further processing after cleaving, referred to as the control; (b) coupons cleaned in Dynastrip AP7880-C, 60 min, 70°C; (c) coupons cleaned in CoatsClean ER105, 60min, 70°C; and (d) Coupons cleaned in XP02028DD, 60 min, 70°C. All coupons were cleaned using an immersion beaker process with agitation similar to recirculation in a tank. Solution heating was controlled by temperature feedback and slow agitation in the beaker. Once the cleaning interval was complete, the coupons were removed, rinsed with deionized water and dried. Analysis was completed on the solution by ICP, PVD blanket Cu coupons to determine Cu etch rates, and Si3N4 and SiO2 blanket coupons to determine nitride and oxide loss. TSV cleaning and particle re-deposition was determined using:
(1) optical microscopy using a Nikon LV150;
(2) scanning electron microscopy (SEM) using an FEI Helios dual beam microscope equipped with an EDAX energy dispersive x-ray (EDX) analyzer; or a Hitachi SEM; Samples were prepared for SEM imaging by depositing a coating of Au/Pd using a Desk II Denton Vacuum Bench top PVD system. The sample was sputtered for 100s using a Au/Pd target, 4” diameter, 1/8th inch thick, to deposit approximately 0.8nm of PdAu.
(3) Auger Electron Spectroscopy (AES) was performed using a Physical Electronics 680 Scanning Auger Microprobe. The data was collected using a 10keV, 10nA electron beam which contacted the sample at 30° from sample normal. The samples were mounted on a stainless

steel puck and placed in the system load-lock. Clean tweezers and gloves were used for all sample handling. No additional cleaning steps were implemented. After sufficient evacuation, the sample puck was inserted into the analytical chamber and placed in front of the analyzer. Secondary electron imaging was used to locate and record areas of analysis. The quantification of the elements was accomplished by using the elemental sensitivity factors.

RESULTS AND DISCUSSION

Silicon wafers were cleaved into ~2.5 x 4 cm2 coupons for beaker scale cleaning tests. The coupons were immersed in heated solutions of Dynastrip™ AP7880-C, CoatsClean™ ER105 and XP02028DD, a new non-TMAH containing post-Bosch process cleaning solution. The wafers were all processed for 60 minutes at 70°C. Post cleaning, the coupons were removed from the solution, rinsed with DI water and dried. Optical images of the wafer coupons before and after clean are shown in Figure 3.

Optical images show a silicon surface with TSVs and free of particles, but do not show details of cleaning. In order to determine details of cleaning, the samples were cleaved to expose the length of some of the TSVs. Analysis was conducted at three sites; top, middle and bottom. Figure 4 shows optical and SEM images of the TSVs across the cleaved end of the samples. The images in Figure 4 illustrate some of the challenges associated with determining the definition of clean for TSV processes. In the images shown, some particles adhered to the silicon surface during cleaving. Other residue is not easy to see visually making it very challenging to observe differences in cleaning between the as-received TSVs (control sample) and the cleaned TSVs, even when viewing the TSV as a cross-sectional image at very high magnification. These types of observations have driven TSV cleans to lower priority in developing 3DIC platforms.

However, the data continues to build support for the need for clean processes to improve reliability and there is also a need to use the right techniques to determine it.4 Standard analytical and surface sensitive techniques used widely in fabs such as optical microscopy and SEM may not provide all the information needed.

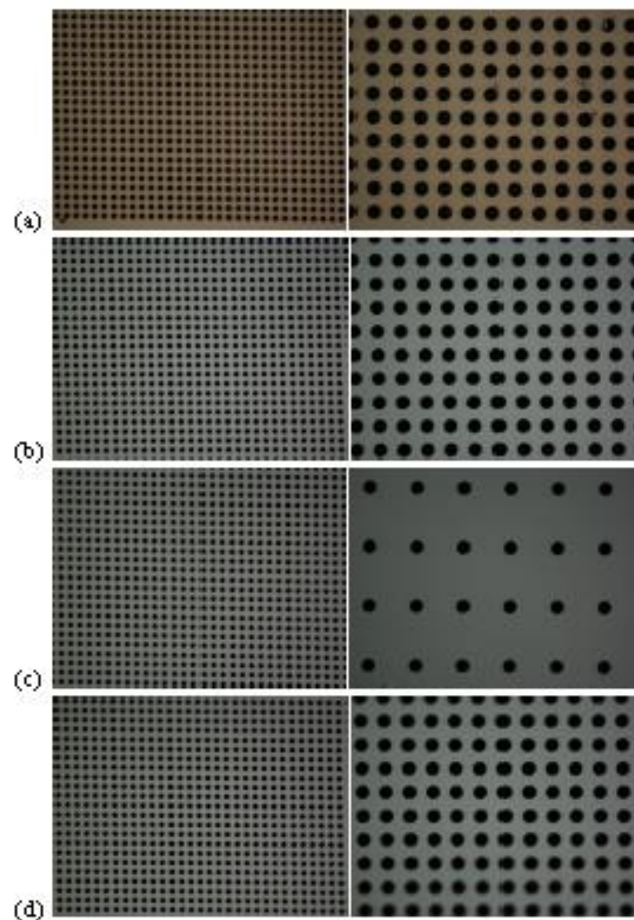

Figure 3. Optical images of wafer coupons 200x and 500x.
(a) Control sample, after DRIE but prior to ashing or additional cleaning process, (b) after cleaning in XP02028DD, 60 min 70°C, (c) after cleaning in CoatsClean ER105, 60 min 70°C, (d) after cleaning in Dynastrip AP7880-C, 60 min 70°C.

Figure 5 shows the surface elemental analysis determined for the above samples using energy dispersive x-ray analysis, EDX. Although the depth of penetration of the EDX beam into the surface can be tuned by optimizing the beam energy and tilting samples at an angle, it is generally accepted that it penetrates into Si samples ~ 2µm for top down measurements and using a 15keV beam energy. For residue that is only 10's of nanometers thick, the signal may be dominated by the signal due to the substrate in the 2µm sampling depth. A more surface sensitive technique, such as Auger spectroscopy (AES) must be used.

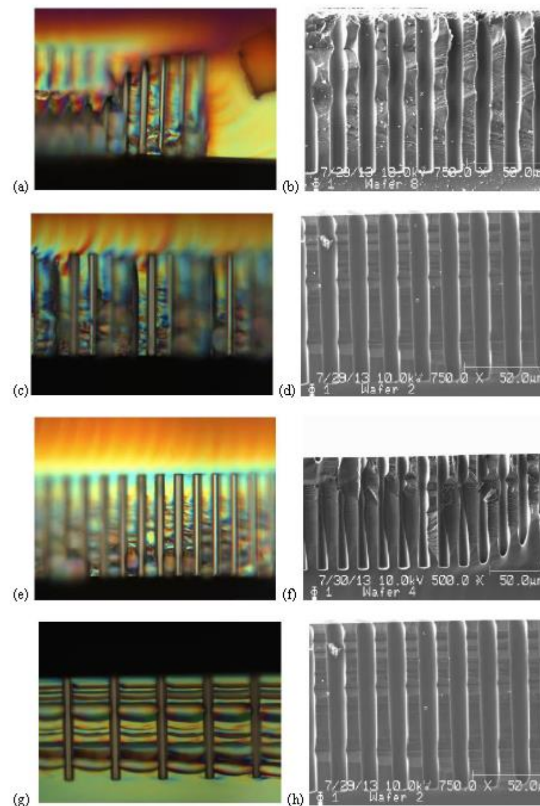

Figure 4. Optical images, 500x, and SEM images, 750x of cleaved TSVs (a, b) control sample, after DRIE, without ashing and before cleaning, (c, d) TSVs cleaned using XP02028DD, 60 min at 70°C, (e, f)TSVs cleaned using CoatsClean™ ER105, 60 min 70°C, (g, h)TSVs cleaned using Dynastrip™ AP7880-C, 60 min 70°C.

Auger spectroscopy is a very suitable surface technique for resolving compositional information at areas near the solder bump since the analysis spot size is small and the depth of penetration (4 – 50 Å) is very low, enabling analysis of small and high density features. Currently, tools that can inspect whole wafers in a non-destructive manner exist, although even with stage tilting capability, they are limited to the top of the TSV sidewall. For spectra to be generated, a photoelectron beam must be able to interact with the surface and then the ejected Auger electron must be captured by the detector. In deep TSVs it is difficult for the Auger electron to escape from the via for the detector to detect it. For tools that can be tilted, measurements can be made at the top of the sidewalls, but analyses at points along the sidewall towards the bottom of the via, particularly for small diameter vias, are not possible. As a result, sacrificial cleaved samples are analyzed to generate spectra such as those provided in Figure 6, and they are used to determine cleanliness. The learning is applied to whole wafer processes.

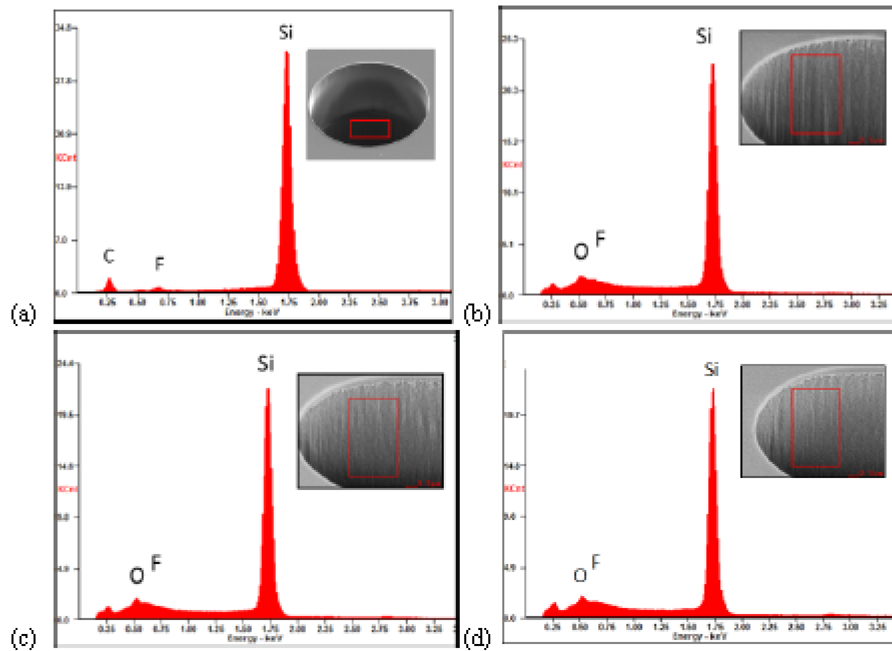

Figure 5. EDX spectra of cross-section TSV coupons (a) control sample, after DRIE but without ashing and before any additional cleaning process, (b) after clean using XP02028DD, 60 min 70°C, (c) after clean using CoatsClean ER105, 60 min 70°C, (d) after clean using Dynastrip AP7880-C, 60 min 70°C.

Typical results, shown in Figure 6, were obtained for each sample described above. For each case, two TSVs were analyzed in three (3) positions indicated by the circles on the SEM image. A red circle indicates a TSV sidewall position close to the surface of the silicon, a blue circle indicates a TSV sidewall position about mid-way or about 50μm from the top of the silicon or the bottom of the via, and the turquoise circle indicates a position at the bottom of the 100μm via. The size of each peak in the scan is proportional to the amount of the element that is present in the sample, provided that there is no peak overlap. For these analyses, the unique binding energies of interest were silicon (Si, 1621eV); oxygen (O, 510eV); carbon (C, 275eV); and fluorine (F, 659eV). Some sample charging was caused by the formation of silicon oxides (SiOx) and the final binding energies were corrected by the standard technique of comparison with the carbon kinetic energy (275eV). Common elements to all the samples included silicon, oxygen and carbon. The elemental concentrations were consistent from one via to the next and from the surface of the silicon to the bottom of the via.

The results shown in Figure 6(a) were recorded using the sample that did not undergo any cleaning processes after TSV formation. The spectrum shows the presence of carbon, oxygen, silicon and fluorine. Fluorine was deposited as a component of the passivation layer formed during the DRIE process using C3F8 gas. The presence of fluorine was used as the most

important indicator of removal of the etch residue. Removal of carbon as an indicator of residue removal is made difficult by the presence of adventitious carbon in the vacuum chamber, which cannot be removed. The AES technique cannot distinguish between carbon from the residue and adventitious carbon. As a result, samples were considered clean when there was no peak from fluorine and the carbon peak had decreased in size. Figure 6 (b-d) show spectra of TSVs after cleaning. In each case, the signal for fluorine was removed at the top and middle via analysis points. In the case of Dynastrip AP7880-C, a very small amount of fluorine was found at the bottom of the via. Quantification of the components in the Auger spectra was shown in Table 1. Since Dynastrip AP7880-C has been used commercially for DRIE removal, has been proven to offer a robust automated process and the amount of fluorine at the base of the via was very low, the conclusion was that this sample's incomplete cleaning was due to issues related to manual coupon scale processing. Results for CoatsClean ER105 were consistent with commercial results: complete removal of the etch residue. The complete removal of post etch residue clean result obtained using the non-TMAH formulation, XP02028DD indicated that it may remove DRIE etch residue as well as or better than successful commercial solutions.

SUMMARY

A robust cleaning solution for one step removal of both the photoresist and sidewall polymer residues from TSVs in an immersion process was shown. The new non-TMAH containing post-Bosch process cleans formulation was shown to remove DRIE etch residue composed of carbon and fluorine as well as or better than successful commercial solutions.

ACKNOWLEDGEMENTS

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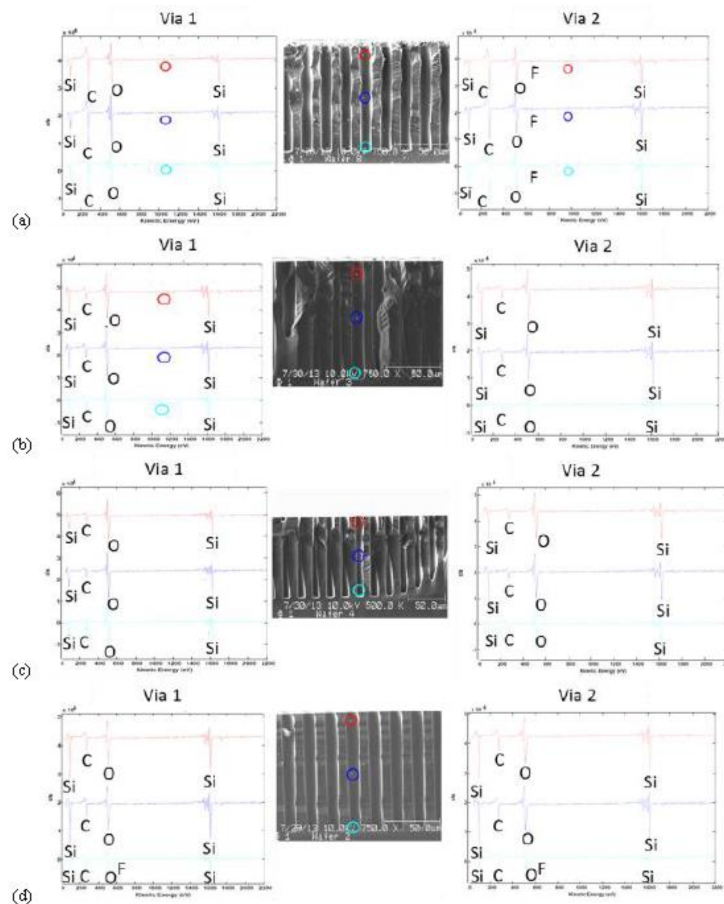

Figure 6. Auger electron spectra and areas of analyses for the same coupons. Results were obtained on two (2) vias to provide additional validation and each via was analyzed in three (3) positions: top, mid way, and bottom. (a) control sample, after DRIE but without ashing and before any additional cleaning process, (b) after clean using XP02028DD, 60 min 70°C, (c) after clean using CoatsClean ER105, 60 min 70°C, (d) after clean using Dynastrip AP7880-C, 60 min 70°C.

Table 1. Tabulated quantification of the components in the Auger spectra.

Sample	atom % C	atom % O	atom % F	atom % Si
Control				
Via 1, Area 1	49	16	0.5	35
Via 1, Area 2	45	17	0.4	38
Via 1, Area 3	48	15	0.8	36
Via 2, Area 1	49	15	0.4	36
Via 2, Area 2	44	15	0.4	40
Via 2, Area 3	50	14	0.5	36
XP02028DD				
Via 1, Area 1	18	26	-	56
Via 1, Area 2	20	25	-	55
Via 1, Area 3	26	24	-	50
Via 2, Area 1	15	23	-	62
Via 2, Area 2	18	22	-	60
Via 2, Area 3	22	23	-	54
CoatsClean ER105				
Via 1, Area 1	18	29	-	53
Via 1, Area 2	15	28	-	57
Via 1, Area 3	28	24	-	47
Via 2, Area 1	16	24	-	59
Via 2, Area 2	15	24	-	61
Via 2, Area 3	25	22	-	53
Dynastrip AP7880-C				
Via 1, Area 1	19	24	0.2	57
Via 1, Area 2	19	23	0.2	58
Via 1, Area 3	39	21	0.8	40
Via 2, Area 1	23	19	0.2	58
Via 2, Area 2	22	19	0.2	59
Via 2, Area 3	35	18	0.4	46