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A Multi-layered Approach for Application of CVD Diamond Heat Spreaders for Cooling of High Power Density (HPD) ASICs

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ABSTRACT

Relative to ceramic heat spreaders, CVD diamond delivers greater benefits for a diverse range of applications and industries [1]. For semiconductor packaging applications, the thermal conductivity of CVD diamond heat spreaders is far superior to any other material available. Significant improvements in thermal management of electronic systems can be realized by using CVD diamond heat spreaders. Integration is relatively straightforward, as CVD diamond can be a direct replacement for aluminum nitride (AlN), beryllium oxide (BeO), or other advanced ceramics and refractory metal/copper matrix.

This paper presents a new approach in which CVD diamond is combined with other heat spreaders. The performance of the combination thermal spreader is evaluated using a parametric model of the temperature field in steady state and in transient operation for a simplified high power multiplexing silicon ASIC (Application Specific Integrated Circuit) by varying geometry, power and thermal properties.

1. INTRODUCTION

In the first part of this work we present a brief summary of the fabrication technology for making and using CVD diamond heat spreaders.

In the second part, using COMSOL Multiphysics® software, the impact of spreading stack geometry, surface flatness, material thermal conductivity and solder uniformity on device temperature is modeled and evaluated [2]. The model evaluates a silicon ASIC device attached to a diamond heat spreader and a corresponding solder layer, a second diamond or other heat spreader and a second corresponding solder layer and a final heat spreader layer with a final solder layer. A COMSOL parametric finite element model allows easy modification of the geometry of the ASIC – thickness, number of hot channels, dimensions, packaging geometry, etc. – material properties and power conditions.

Material properties have been extracted from literature results and/or modeled using published methods.

2. CVD DIAMOND HEAT SPREADER

Diamond synthesis

Deposited from a mixture of hydrogen and carbon precursors, a typical microwave CVD diamond growth process is carried out in a vacuum chamber onto a suitable substrate and at a fraction of atmosphere [1]. Energy derived from a microwave source is used to dissociate molecules of precursor gases to form diamond on the surface of a substrate [3]. Typical carbon precursor gases are hydrocarbons such as methane (CH_4) with the possible use of other carbon precursors such as carbon monoxide (CO) in some synthesis recipes. Typically, the ratio of carbon precursor to hydrogen [CH_4]:[H_2] is of the order of a few percent. Substrate temperatures during the deposition process are between 550°C and 1200°C, and deposition rates are usually measured in micrometers per hour.

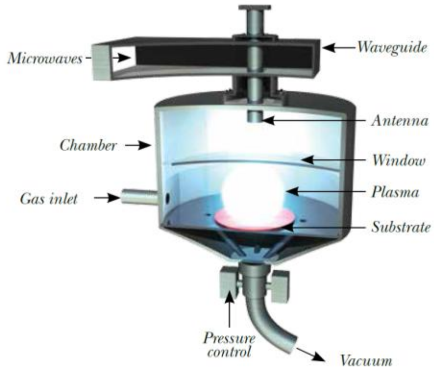

Figure 1: Schematic of a typical microwave plasma assisted CVD diamond reactor

Shaping diamond heat spreaders (lapping, polishing and laser cutting)

Synthesizing CVD diamond covers only half of the engineering technology used to manufacture CVD diamond heat spreaders. Post-synthesis processing covers the other half (Figure 2). These steps involve rough and fine lapping of diamond substrates, followed by polishing and laser cutting of the material to achieve the final specifications and shapes. Through novel techniques and advanced engineering practices, diamond heat spreaders can be formed with exceptional dimensional tolerances and specifications:

- Planar dimensional tolerance = -0.0/+0.1mm
- Thickness tolerance = ±0.050 mm
- Polished surfaces: Ra < 10 nm
- No more than ± 10 nm variation of Ra (over 25 mm diameter)
- Flatness < 0.010 mm (over 25 mm diameter)

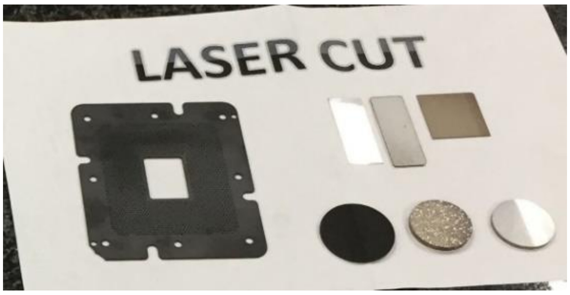

Figure 2: Examples of lapped, polished and laser cut diamond wafers and specimens

Laser machining of diamond is achieved through thermal ablation or laser-assisted chemical etching in oxygen or air. Laser drilling and cutting of diamond could be in single or multi-step processes. It typically involves high-energy thermal conversion of the top surface to graphite, followed by ablation of converted graphite and the forming of another thin layer of graphite. The thickness of this graphite layer depends on pulse duration and the thermal conductivity of diamond. In some cases, it might be advantageous to coat the diamond with specific layers for better profile and dimensional control.

Metallization and mounting of diamond heat spreaders

Sputtered refractory metals such as titanium and chromium can form highly adherent and chemically bonded connections with CVD diamond. In combination with a final gold layer they provide an ideal metallization stack for most electronics and optoelectronics applications [4]. To ensure chemical stability at higher operating temperatures the gold and titanium layers are physically separated by a sputter-deposited thin barrier layer of platinum or titanium-tungsten (TiW). The typical thickness of this barrier layer is usually around 80-200 nm.

Depending on the application, the gold layer thickness could be anywhere from 500 nm to 2-3 µm. Figure 3 shows an example of CVD diamond heat with patterned metallization.

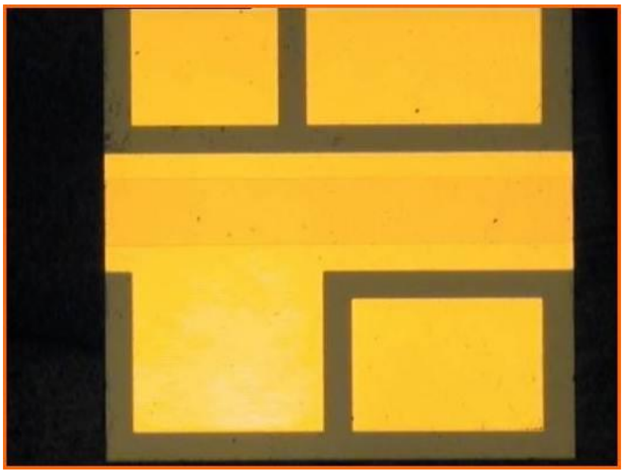

Figure 3: Metallized and patterned CVD diamond heat spreader

3. COMSOL MODEL FOR HEAT SPREADING

Our model consists of three sections:

1. A section where the geometry and material properties of each component of the design are defined
2. A section where the geometry, mesh and simulation are created and visualized
3. A log showing the information about the progress and details of the different simulation steps

The geometry section consists of four subsections that are as follows:

Silicon ASIC: In this subsection the thickness of the ASIC and the number of channels and their dimensions are defined. The thermal conductivity, heat capacity, density and the corresponding temperature adjusted values are extracted from the literature (Fig. 4).

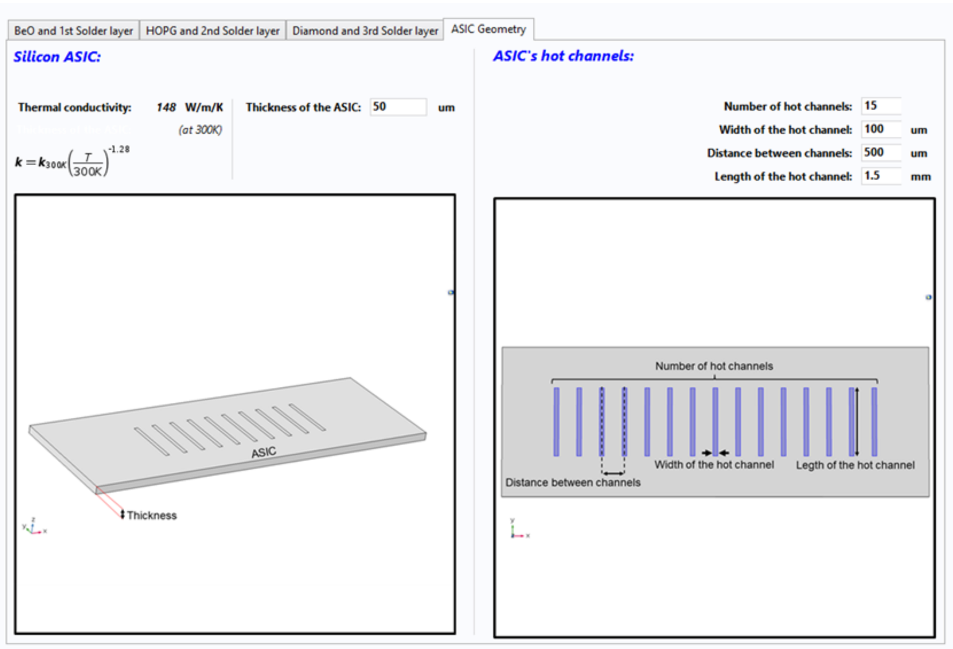

Figure 4: Design and properties of the ASIC

Diamond heat spreader: The dimensions of the diamond heat spreader and the connecting diamond/ASIC solder layer are defined in this section. The solder is defined as a plane using three points, thus allowing for tilted planes to evaluate the impact of solder thickness non-uniformity. Material properties for the solder are extracted from literature. Diamond material properties are sourced from both literature and from Element Six proprietary data.

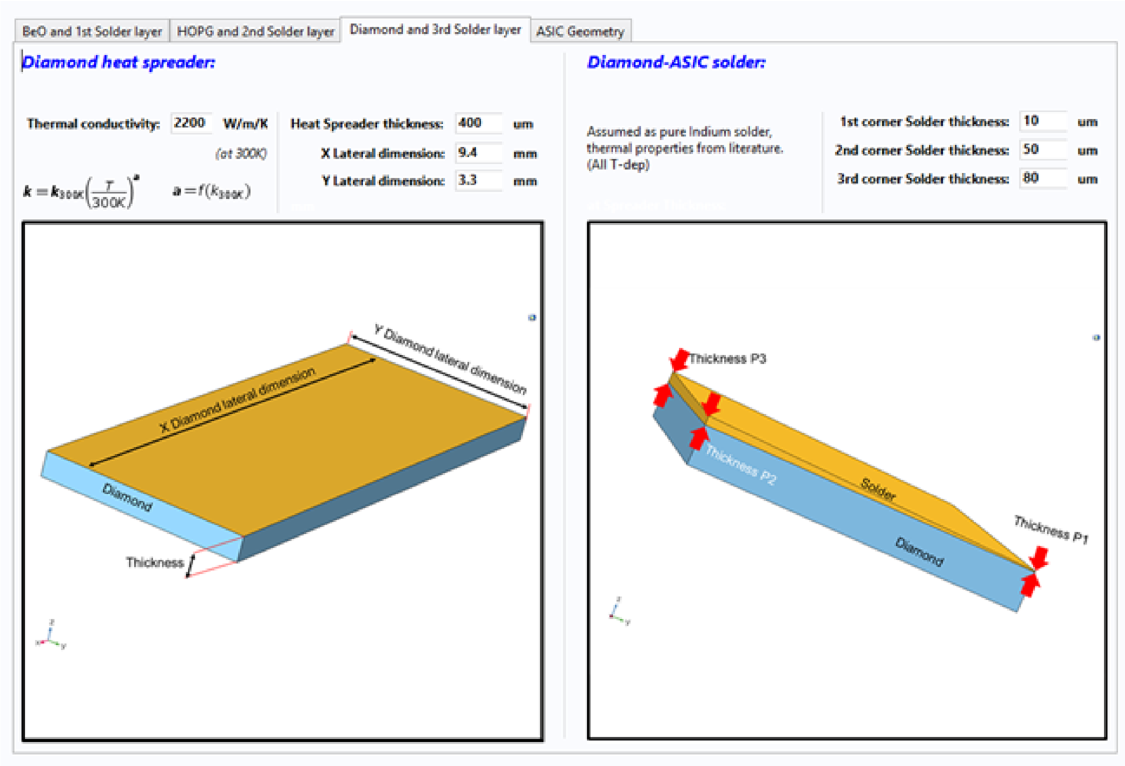

Figure 5: Design and properties of the diamond heat spreader and solder attachment between the ASIC and the heat spreader

Second and third heat spreaders: The geometry and properties of the second and third heat spreaders along with any corresponding solder layers are defined in this section. The second (Fig. 6a) or third (Fig. 6b) heat spreader could be lower thermal conductivity CVD diamond, highly oriented pyrolytic graphite (HOPG), BeO, AlN or any other combination of heat spreader attached to heat sinks. They could be oversized (Fig. 6) to allow for in-plane thermal spreading away from the primary CVD diamond heat spreader to the first heat sink or heat pipe.

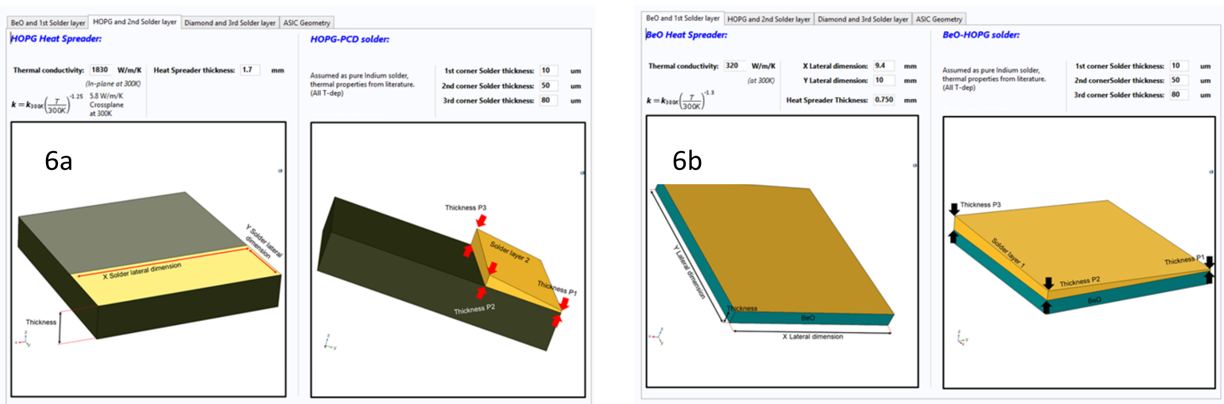

Figure 6: Design and properties of the second and third heat spreaders and solder attachments

4. STEADY STATE CASE STUDIES

Solder uniformity - Case study

<u>Case 1:</u> We studied 15 channels at 10 W per channel. Channel dimensions were at 0.1 mm width, 1.5 mm length with a 0.5 mm channel to channel pitch. The silicon ASIC thickness was fixed at 80 µm and three solder layers between ASIC, diamond, second spreader and final sink/spreader all at 50 microns in thickness. The heat spreader stack consisted of 400 µm of 2000 W/mK diamond heat spreader one, 1.7 mm thick pyrolytic graphite heat spreader two with in-plane thermal conductivity of the order of 1600 W/mK and a final heat sink/spreader of 0.750 mm thickness and thermal conductivity of the order of 250 W/mK (Fig. 5).

<u>Case 2:</u> Same as Case 1 with diamond/ASIC solder having two corners at a thickness of 10 µm and two corners at the nominal thickness of 50 µm. The other two solder layers are assumed to be uniformly 50 microns thick.

Figure 7 shows the temperature field for both cases. The model clearly predicts the impact of thinner solder at corners on the peak temperature as well as any induced non-uniformity in the temperature. The channels closer to where the solder is thinner show a lower peak temperature compared to where the solder thickness is homogeneous.

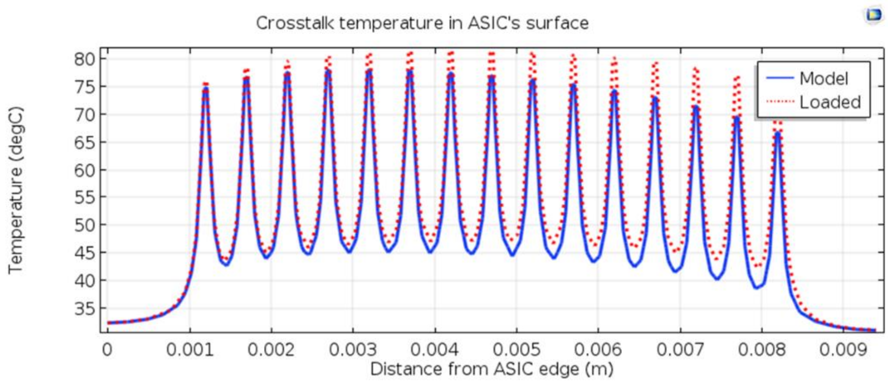

Figure 7: Crosstalk temperature for the ASIC

Impact of better heat spreader on solder non-uniformity - Case study

<u>Case 3:</u> The simulation for 10 channels at 15 W per channel placed on 500 µm of CVD diamond heat spreader at 1500 W/mK, attached to pyrolytic graphite heat spreader atop of heat sink with uniform solder thickness at 20 µm at all level results in maximum peak temperature at 104°C.

<u>Case 4:</u> The simulation for 10 channels at 15 W per channel placed on 300 µm of CVD diamond heat spreader at 2000 W/mK, with the same pyrolytic graphite heat spreader atop of heat sink with non-uniform solder at 20, 50 or 70 µm at solder level 1 results in maximum temperature at 106°C.

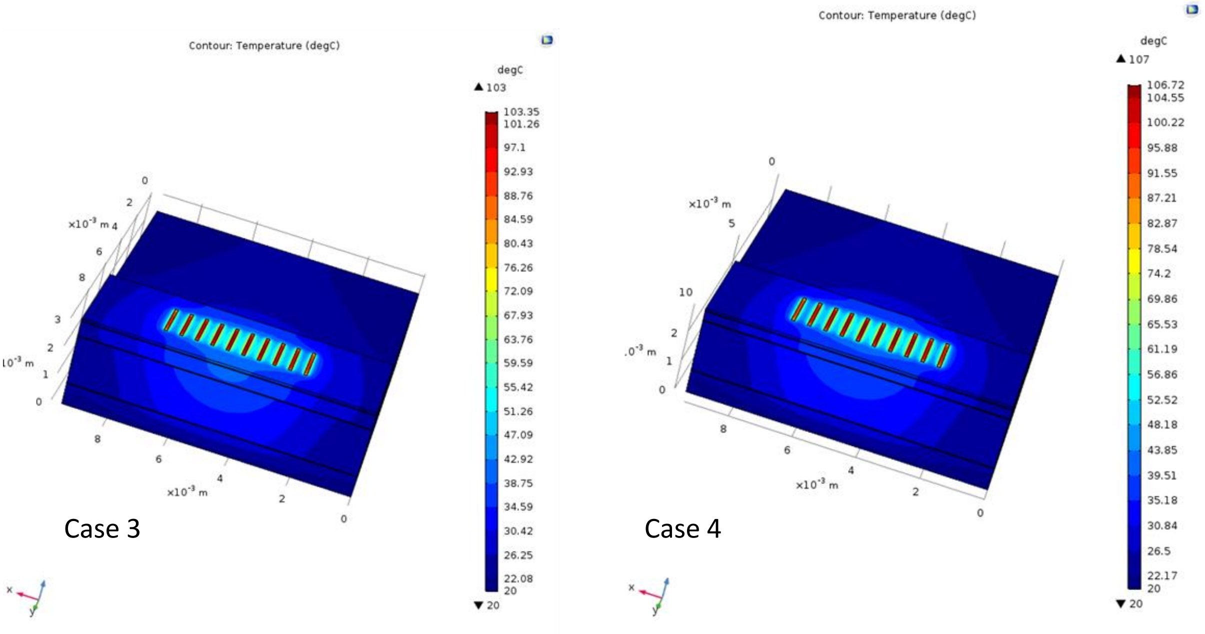

Figure 8: 3D steady state simulation results on impact of better thermal conductivity on poor solder uniformity

The review of these two case studies are represented in Figure 8. Simply stated, using higher thermal conductivity CVD diamond heat spreader helps to reduce peak temperature rise caused by solder thickness non-uniformity.

Impact of channel pitch and channel

Case 5: A simulation for an ASIC with 10 channels operating at 10 W per channel at 0.7 mm pitch mounted on a triple stack of CVD diamond on pyrolytic graphite on a CuMoCu heat sink was undertaken to evaluate the impact of CVD diamond thermal conductivity not just on maximum temperature, but the impact of cross talk between channels. In one case (5a), CVD diamond thermal conductivity was kept at 2200 W/mK. In case (5b), CVD diamond thermal conductivity was reduced to 700 W/mK.

Case 6: A simulation similar to Case 5 with the exception of an ASIC having 20 channels operating at 10 W per channel at 0.4 mm pitch was studied. It showed that irrespective of power density, a higher thermal conductivity CVD diamond heat spreader will not only reduce the maximum temperature, but also reduce the cross talk related temperature rise.

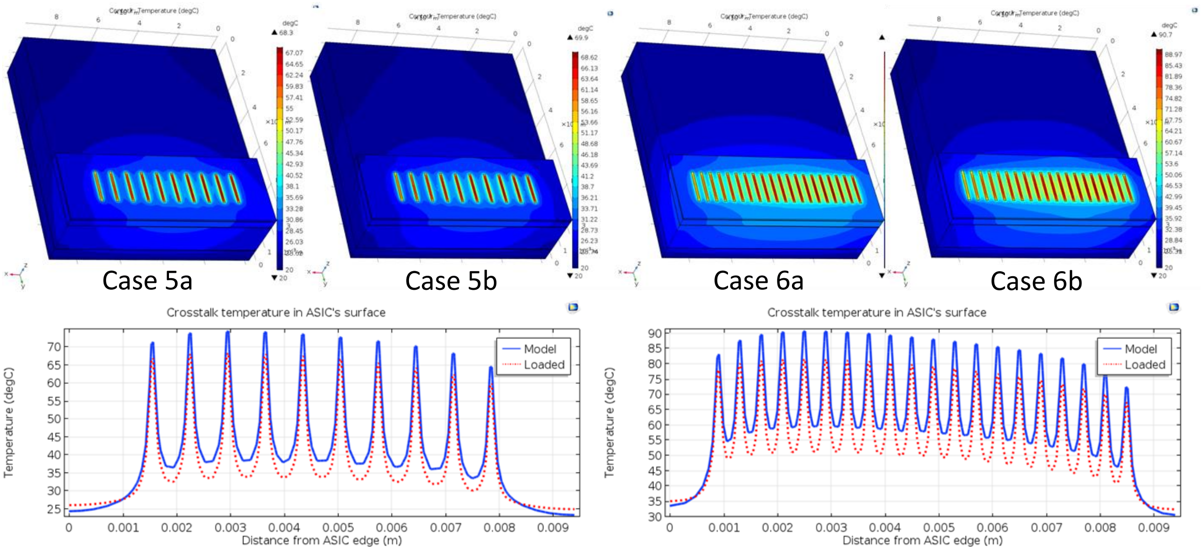

Figure 9: 3D steady state simulation results on impact of better thermal conductivity on channel density

5. SUMMARY

A model created in COMSOL Multiphysics® was used to study an approach in which CVD diamond is combined with other heat spreaders to passively cool high power density silicon ASICs. The peak temperature rise, as well as temperature field profile and the impact of cross talk between hot channels was characterized as a function of geometry, material properties and solder uniformity.

6. REFERENCES

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