ORIGINALLY PUBLISHED & PRESENTED AT ECTC 2019

Vertical laser assisted bonding for advanced "3.5D" chip packaging

Andrej Kolbasow, Timo Kubsch, Matthias Fettke, Georg Friedrich and Thorsten Teutsch
PacTech GmbH
Am Schlangenhorst 7-9, 14641 Nauen, Germany
Phone: +49 (0)3321 4495-504, Fax: +49 (0)33214495-110, E-Mail: fettke@pactech.de

***Abstract* — In this work the processes of laser assisted bonding (LAB) is compared to thermal compression bonding (TCB). Their respective advantages and disadvantages regarding the assembly of flip chip stacks are compared. It is found, that the LAB allows for faster processing, negligible compression force and creates less internal stress in the chip stack. The concept of "3.5D" stacking is introduced. This new concept allows for the vertical bonding of chips/semiconductors to the sides of a chip stack. The vertically bonded parts can be used to contact the individual layers, which eliminates the necessity for through silicon vias (TSVs).**

Keywords - *3D-packaging, Laser assisted bonding (LAB), Thermal compression bonding (TCB), Silicon interposer, System on Package (SOP), Laser beam modulation, Inter metallic phase (IMC-layer), vertical Flip Chip bonding*

I. Introduction

Growing performance, further miniaturization and increasing system density are major technical drivers for the global semiconductor market to improve and develop new chip-designs and packaging-concepts. 3D-IC and 2.5D TSV (through silicon via) packaging technologies are common concepts of tackling this challenge by manufacturing multi-layer packages such as HBM (Hight Bandwidth Memory) and HMC (Hybrid Memory Cube). Caused by the continuous demand of increased performance, density of interconnects such as TSVs, micro bumps and Cu pillars between and inside of each layer increases significantly. Parasitic effects such as capacitance, inductance, resistance and EMI (electromagnetic interference) compatibility bring daily challenges for developing new packaging concepts, designs and manufacturing technologies [1]. Beside design and concept challenges, economic and reliable manufacturing technologies play an important role by achieving new technological standards. In this study we will introduce new, economic and reliable concepts, to bond vertical semiconductors against a chip package at all four sides to build a new "3.5D" chip package (see Figure 1).

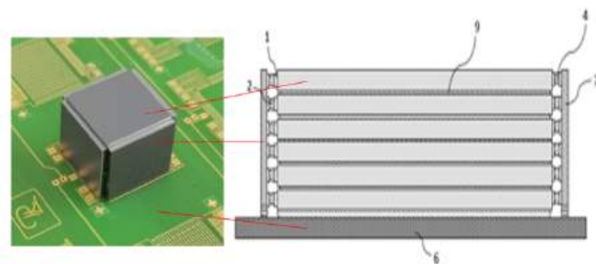

Figure 1: Stack with vertically bonded semiconductor devices.

The major goal is to redistribute TSV structures to the die edges and realize the layer interconnects via vertically bonded chips.

The presented assembly technology enables the possibility to use interconnects at the die edges or top / bottom combination and gives future designers the possibility to reduce or eliminate interconnect density from die main area and move it to the package edges. Die layouts can be simplified and parasitic effects of interconnects minimized. In this study, metrology comparison of generated interconnects by TCB and LAB process will be shown. Shear-tests, cross-section, X-ray, EDX and thermal aging analyses will provide reliability data for further discussions. Finally, the concept of "3.5D" stacking will be outlined and first assembly results presented.

II. Materials and Test Components

For the performance characterization of the two different bond technologies discussed in this work the test materials presented in Table 1 were selected for qualification tests.

	Description	Picture	Specification
Sample A	Si- interposer		Size: 14mm x 14mm x 110µm UBM: ENIG Type: interposer for SOP applications
Sample B	PCB		Size: 20mm x 20mm x 1mm UBM: ENIG Type: Multilayer PCB
Sample C	Si Pac Tech test die		Size:14mm x 14mm x 110µm UBM: ENIG Type: Pac Tech Silicon Test Die
Sample D	Si Pac Tech test die		Size:14mm x 14mm x 110µm UBM: ENIG Type: Pac Tech multi project PCB board
Material A	MEMS		Size: 0.3mm X 0.3mm X 190µm UBM: ENIG Type: MEMS
Material B	SAC 305 Solder balls 250µm - Solder preform		Size: 350µm +/- 5µm Melting point: 493.15K Alloy: Sn96.5% Ag3% Cu0.5%

Table 1: Substrate and material overview.

III. Process Description of Chip Bonding Technologies

A 3D-axis system, a bond chuck and a bond tool are a bonding system's central basic components. The common goal is the realization of a reliable interconnection between two substrates. The main difference between laser assisted bonding and thermal compression bonding is the mechanism of inducing the required energy into the devices for sufficient soldering.

Before the bonding sequence is started, the daughter substrate is picked up by the bonding unit via vacuum, optically measured and finally aligned to the mother substrate located on the bond chuck.

A. General process flow of PacTech's LAB system (laser assisted bonding)

A modulated near infrared laser beam is used to heat up the daughter substrate to be placed on the mother substrate. At its bottom, the daughter substrate features a set of pre-soldered interconnects, which are wetted with flux (see Figure 2).

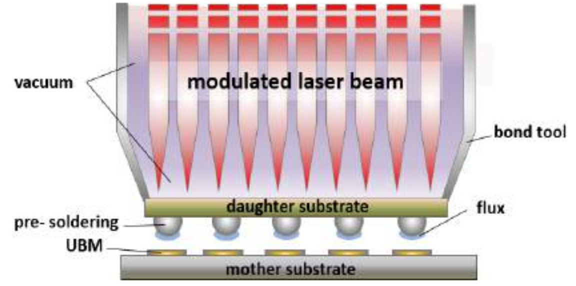

Figure 2: Basic process setting of PacTech`s LAB bonding process.

In this particular case, the beam modulation is performed in two steps. Step one is the transformation of the initial gaussian profile into a top-hat profile. In step two, the beam is resized into the desired shape by means of an adjustable, rectangular aperture (see Table 2).

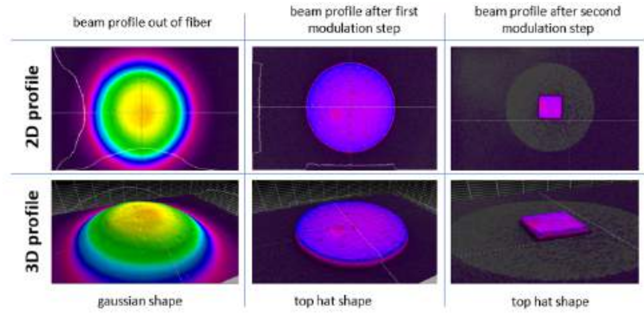

Table 2: Basic illustration of laser beam modulation.

Size, shape and energetic homogeneity of the laser beam are depending on the optical configuration of the used lens system. The modulated laser beam passes through the aperture of the ceramic bonding tool. During the bonding process, a force and IR sensor monitors and records the process conditions in order to keep the process parameters in the defined process range. A positive thermal gradient over time of up to 1773.0K/s within a ±0.3K range can be achieved based on the component size and material. Before the component to be placed touches the mother substrate, the solder is liquefied by the energy thermally induced by the laser beam. Finally, the component is placed on the mother substrate and bonded. No significant force is needed, since the solder is liquefied before touchdown [2, 3].

B. General process flow setting of a TCB system (thermal compression bonding)

An electrical coil is used to heat a ceramic or metallic bonding tool. The principle configuration of a TCB bonding setup is illustrated in Figure 3.

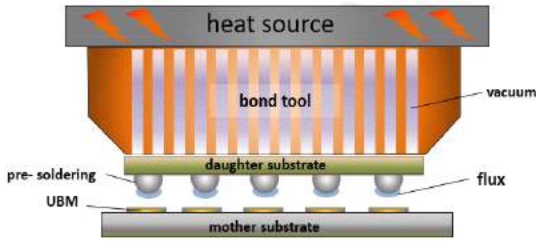

Figure 3: Process setting of TCB bonding unit.

The heat distributes throughout the tool, which then heats the component to be placed. The quality of the heat distribution depends on the tool design, size and material. During the approach, the component is kept below the melting temperature of the solder. A force sensor is used to detect the touchdown at substrate surface before increasing the heat to liquefy the solder that is already in contact with the mother substrate. Heat ramping speeds of about 473K/s are possible. Due to thermal losses at the heated bond tool, an offset calibration is continuously necessary before and while bonding [8,9,10] .

IV. COMPARISON BETWEEN THERMO COMPRESSION BONDING AND LASER ASSISTED BONDING

A. *Investigation of possible warpage effect by bonding Si-interposers on PCB substrate*

In order to analyze and compare possible warpage effects between the TCB and the LAB process, three sets of samples have been assembled for each process (see Table 3). Afterwards samples have been measured using a "Keyence VR 3000" 3D-Profilometer. The results were confirmed using a Keyence LK-G3000 laser sensor. Table 3 describes the test configuration that has been used for sample making. As shown, the main bonding parameters are significantly different between both processes.

	Sample 1	Sample 2	Sample 3
Picture			
Remarks	PCB substrate bonded to one interposer	PCB substrate bonded to two stacked interposers	PCB substrate bonded to three stacked interposers
main TCB process parameter	**Process temperature:** 583,15K **Process time (total):** 20s **Bonding force:** 10N **Pre-heating:** ---	**Tool / component cool down:** N² shower **Flux:** TACFLUX 10- Indium corp.	
main LAB process parameter	**Process temperature:** 513,15K **Process time (total):** 7s **Bonding force:** --- **Pre-heating:** ---	**Tool / component cool down:** no **Flux:** TACFLUX 10- Indium corp.	

Table 3: Test description and specification for substrate warpage evaluation.

The most drastic differences are found in the bonding force, the peak temperature and the process duration. All samples have been pre-soldered by PacTech's SB² (Solder Ball Bumping) solder jet process [4]. Spherical solder preforms with a diameter of 350µm of an alloy of SAC305 (Sn 96.5%, Ag 3.0%, Cu 0.5%) have been used to generate proper solder depots on the interposer pads. On the 190µm octagonal pads a mean solder bump height of 300µm was measured after solder jetting. Table 4 shows solder height deviation after pre-soldering process by SB² on interposer.

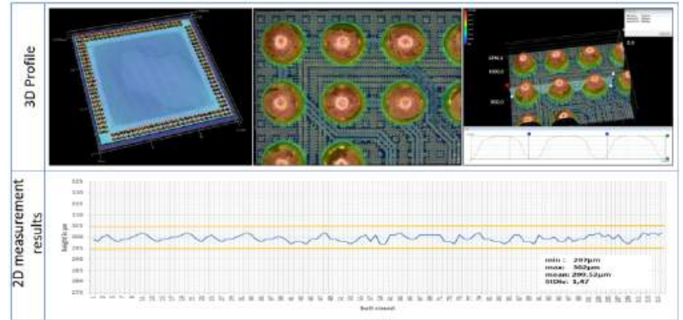

Table 4: Solder height measurement results by 3D profiling and 2D measurement.

After the pre-soldering process, three samples for each of the bonding technologies have been prepared. Figure 4 and 5 show the observed thermal energy profile during the bonding process.

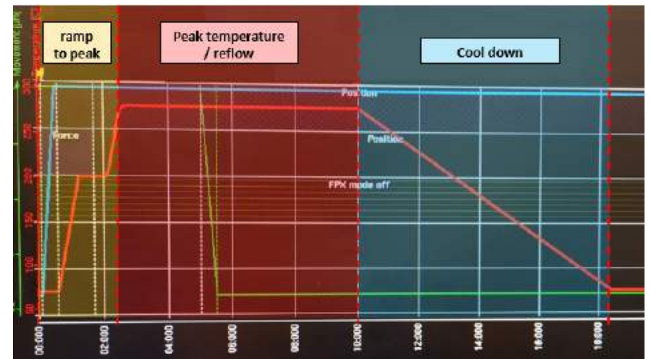

Figure 4: Thermal energy profile during the TCB process recorded by temperature sensor at the tool heating unit.

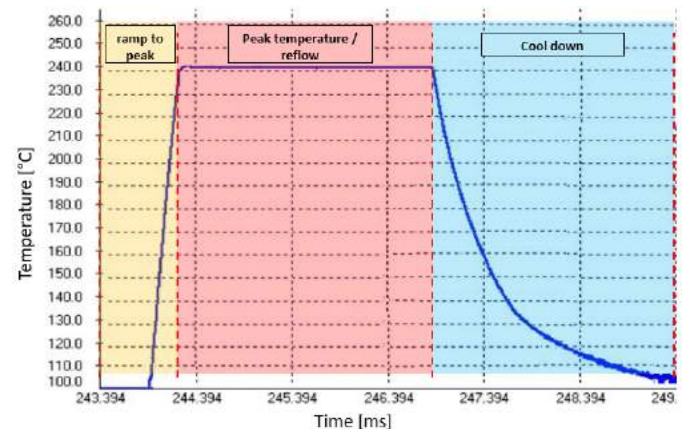

Figure 5: Thermal energy profile during PacTech's LAB process recorded by IR-sensor on device surface.

As shown in Figure 4 and 5, there are major differences in time, ramping speed and cooling characteristic. This is mainly caused by the fashion in which the interposer is heated. During the TCB bonding, the system needs to heat up the mass of the bonding tool in order to heat the interposer. In the LAB

process, the heat is directly created at the interposer surface via interaction with the laser radiation. As described in Table 3, in contrast to the TCB process, the LAB system requires no N_2 for rapid cooling since there is no significant mass to cool down.

It is also to be noted, that the thermal profile displayed in Figure 5 has been measured at the top of the bonding tool. The usual static temperature offset between the top and the bottom of the tool has been taken into account (≈ 67K in the process at hand). The temporary drop in temperature as the warm tool touches the cold sample, can however not be accounted for as the heat transmission through the tool is too slow. In contrast, during the LAB process, the temperature is measured optically, directly at the sample.

A common problem in chip stacking is internal stress and strain in the stack. The stress is created during the bonding process. It is caused by thermal expansion and shrinkage of the component before and after mechanically fixing it to the underlying stack. A less than ideal thermal profile of the process may also negatively influence the amount of internal stress.

The stress can, in combination with mechanical influences such as vibration, lead to the breaking of solder bonds and/or the components in the stack. This can occur at any point in the device's lifetime and needs to be omitted. To investigate the internal stress of a component, its warpage is analyzed.

In order to quantify the warpage, height maps of the top interposer's surface have been taken using the above-mentioned 3D profilometer. The results have then been re-gauged, to let the four corners for each interposer be at height 0. Then the point of maximum elevation was determined, and its height difference to the corners measured.

The Tables 5 and 6 give an overview of the measured warpage in the assembled samples ordered by their number of layers and their bonding method.

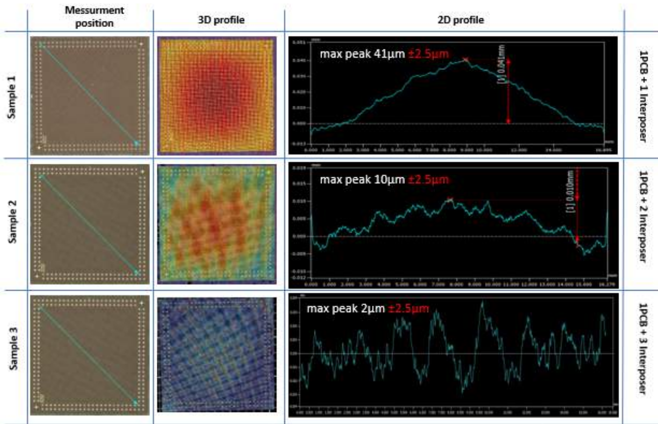

Table 5: Warpage measurement of TCB bonded samples.

For the TCB process a clear surface warpage is identifiable, which shrinks with a growing number of layers in the stack. In the first layer bonded to the substrate, a significant warpage can be seen (see Table 5). While the edges of the chip are fixed to the underlying substrate, its center bulges up by about 40µm in a rotationally symmetric shape. This clearly points at internal stress in the sample and interconnects. In the second layer, the difference is less pronounced and in the third, no significant warpage has been found. As more and more layers are added to the stack, their influences may cancel each other out mechanically, which would lead to the reduction of warpage in the stack. Another explanation may be, that repeated thermal cycling due to the adding of further layers relaxes the components and therefore the stack as a whole. This form of thermal annealing would not only reduce the measurable warpage but also the internal stress causing it.

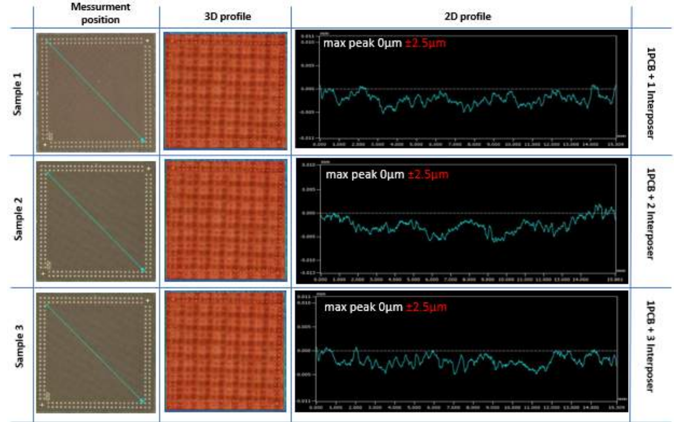

Table 6: Warpage measurement of LAB bonded samples.

In the samples, created using the LAB process, no warpage larger than the measurement uncertainty of ±2.5µm could be observed. To confirm this observation, another set of single layer samples was produced using the LAB and TCB process under identical conditions. This second set was measured as well and shows the same warpage behavior.

B. *Comparison of IMC (intermetallic compound) layer characteristic between TCB and LAB process*

In the following an analysis about the formation and aging of the IMC layers, which form during the TCB and LAB process, is discussed.

IMC formation is an essential requirement for a stable and reliable electrical and mechanical interconnection [5]. However, as IMCs age, they grow and become more brittle, which can cause a variety of problems such as cracks, delamination and reduced conductivity [6].

The resilience of the IMCs created via the different bonding processes against thermal aging is investigated. Therefore, in addition to creating the samples, some of them were also exposed to a temperature cycle ranging from -40°C to 125°C over a duration of 35min. To simulate the aging of the part during its lifetime, each sample underwent the temperature cycle 200 times. This is to provoke the formation of weak spots such as micro cracks or bump lift.

The respective results are discussed below. Table 7 displays an overview over the cross sections of bumps generated via TCB and LAB with a special focus on the IMC layer.

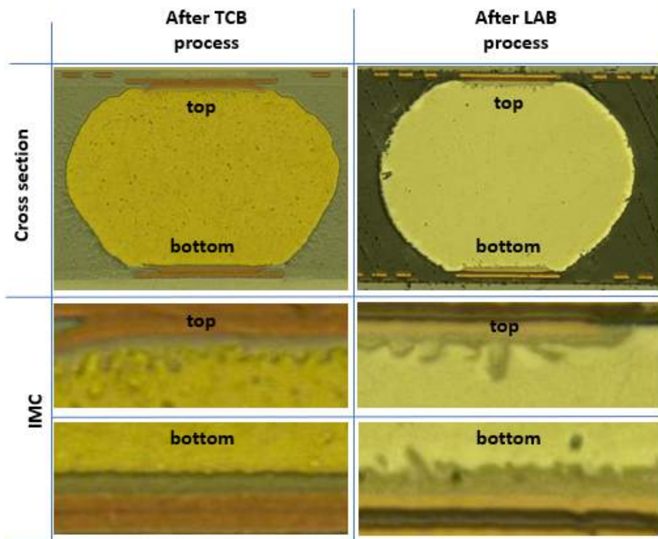

Table 7: Cross-sections of IMC layers of TCB generated bonds.

As can be seen in Figure 6 and 7, two different IMC layers have formed during the TCB process. This is because, in the case of the upper interface, the pre-soldering has been realized using a laser implicit process (PacTech's SB² process). The lower interface was created by the respective bonding process.

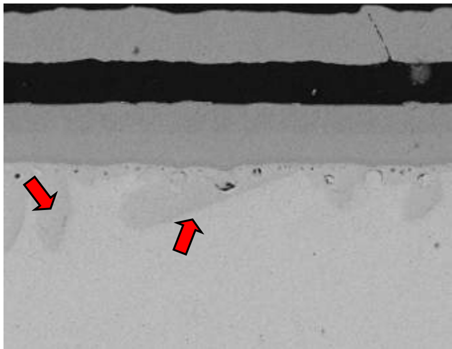

Figure 6: IMC layer of bonds generated by SB² and TCB process (top).

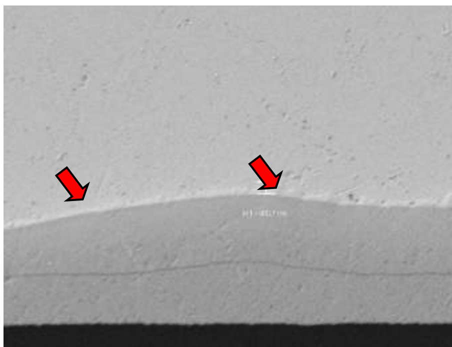

Figure 7: IMC layer of 0.9µm generated by TCB bond process before thermo cycling. (bottom).

In comparison, the IMC produced by only the TCB process are thinner than that with only the SB² process or the SB² and TCB processes combined. The TCB IMCs form a smooth layer, while the ones created by SB² and TCB feature a more acicular structure.

The Figure 7 shows an SEM image of the only TCB IMC after creation and Figure 8 after 200 thermo cycles.

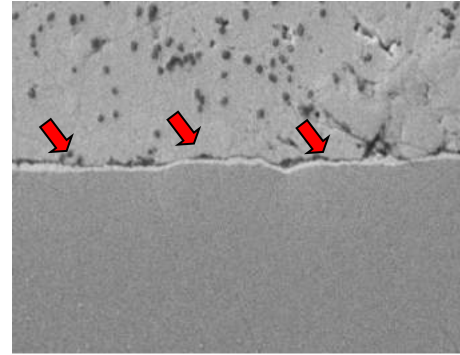

Figure 8: IMC layer of bond generated by TCB process after thermo cycling with micro cracks.

Interestingly, the IMC layers created by TCB have grown significantly more during the thermo cycles than those using the laser implicit process for pre-soldering. While the layer, generated by the only TCB process has grown during the cycling as shown at Figure 9 the IMC layer thickness doubles, the SB² and TCB layer barely changed as shown in Figure 10.

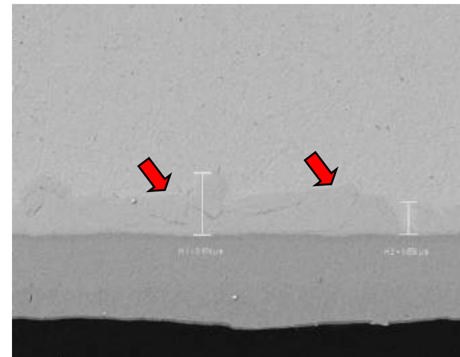

Figure 9: IMC layer of 1.9µm generated by TCB bond process after thermo.

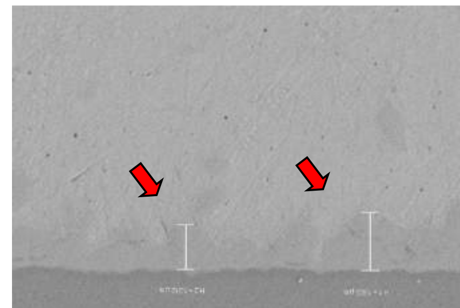

Figure 10: IMC layer of SB² + TCB bond process generated after thermo cycling.

As can be seen in Figures 11 and 12, the IMC's behavior is similar for samples featuring the LAB process with and without the laser implicit pre-soldering before thermal cycling.

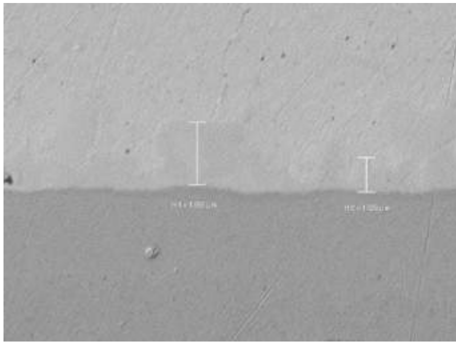

Figure 11: IMC layer of 1.9µm generated by LAB bond process before thermo cycling.

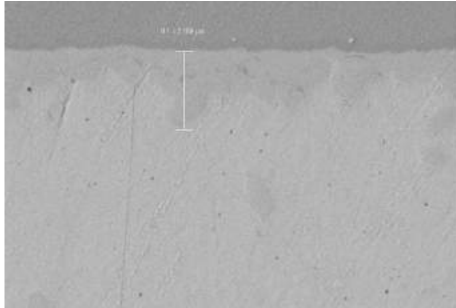

Figure 12: IMC layer of 2.2µm generated by SB² + LAB bond process generated before thermo cycling.

The following thermo cycle test had no negative impact either as shown in Figure 13. No signs of micro cracks or other defects have been found as in the TCB processed ones shown in Figure 8. However, despite these promising results, more reliability tests need to be performed to further investigate the IMC layer created in the LAB process. Based on the data at hand, it can already be assumed, that the LAB process generates a sufficient and resilient IMC layer.

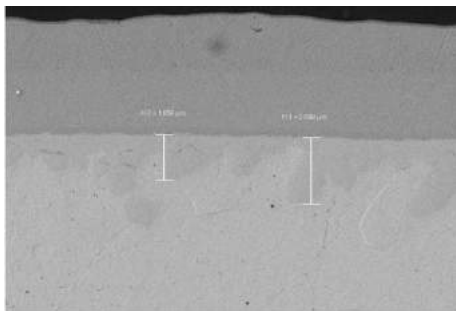

Figure 13: IMC layer of SB² + LAB bond process generated after thermo cycling.

V. Concept of "3.5D" Stacking by Using PacTech's LAB Process

A challenge, besides the prevention of heat spread and parasitic effects inside a complex 3D package with up to 32 layers is the production of reliable TSV interconnects. Most of the layer interconnections of 3D chip stacks are realized by TSV technologies or wire bonding processes. Both ways are cost intensive and include up to 320 process steps (masking, etching, sputtering, etc.). The risk of quality rejects increases with the number of layers and the depth of TSV structures. The realization of a vertical bonding technology for placing active or passive semiconductor elements like interposer devices has the potential to overcome these limitations. "3.5D" stacking technology allows for the reduction or complete elimination of the described challenges as the layers in the stack are contacted using the vertically bonded components and TSVs become obsolete. This does not only create more space on each individual layer, it also allows for more a dense stacking of the layers. All 4 sides of a chip-stack can be used for this vertical placement and bonding.

The prerequisite for the vertical connection of a functional group to a chip stack or chip package is the presence of lateral contact surfaces. These are to be considered and produced in the design and manufacturing of the microchip. Ideally, all of the otherwise on-surface contacts of a microchip may be routed to the side surface. This is extremely advantageous in further reducing the assembly height, since the contact surfaces, built-up of pillars or solder bumps, can be omitted.

The thickness of the stacked chips as well as the minimal pitch of the vertically bonded component are then the limiting factors for the clearance between the layers in the stack.

If this approach is projected onto a wafer production chain, TSV structures are etched along the chip edges in a first step. These are metallized together with the contact conductor tracks, thus creating the contact pad in the form of a TSV.

The chip stack is then fixed to the carrier substrate while the required heat is provided via laser from the bottom of the substrate. The illustrated LAB process, optimized for soldering the stack as a whole to the substrate, is particularly suitable for this step.

The wafers are bonded to each other after thinning and mated using a thin film to form stacks with an arbitrary number of layers. Subsequently, the wafer stack is sawed along the TSV structures and the chip stacks are separated. These stacks can now be connected to a vertical functional module (see Figure 14).

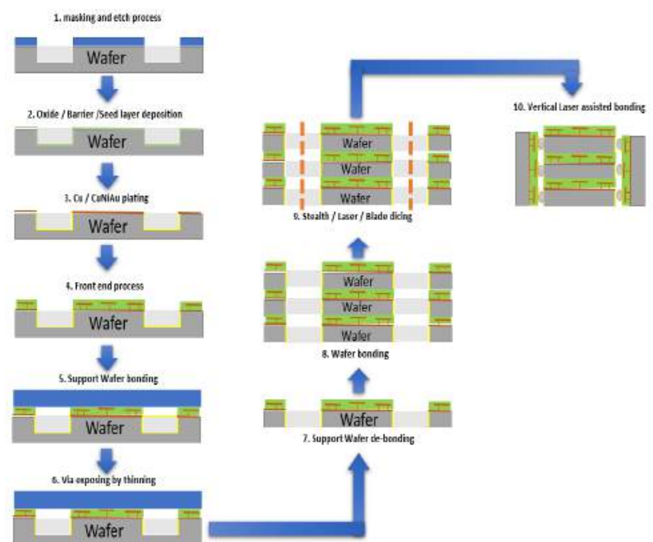

Figure 14: Possible process chain for vertical laser assisted bonding [7].

Like in the sections II and III, where the principles of the LAB and the TCB process have been explained respectively, the concept of the vertical chip bonding will be outlined in this section using a process example. Figure 15 shows a schematic representation of the process.

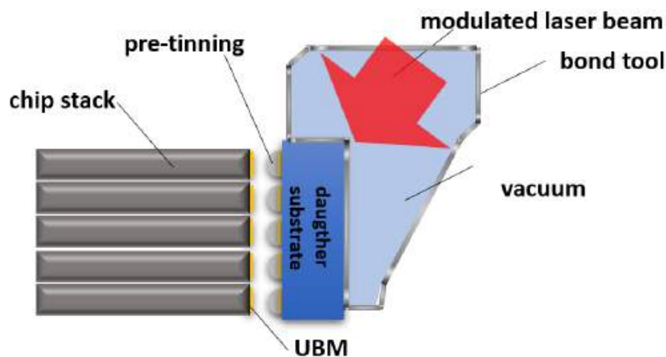

Figure 15: Schematic representation of the vertical chip bonding process.

For the initial assembly tests of vertically bonded components at the sides of a "3.5D" chip stack, the LAB process is used. This is mainly because it has a smaller thermal impact on the assembly as a whole. The bonding system performing the task is PacTech's "Laplace-Bonder". The optic imaging system, as well as the tooling, have been redesigned and adapted to fulfill the requirements of a 45° orientation. A special transfer station allows for the handover of the horizontally stored chip to the 45° tilted tool. A vacuum is created inside the tool to fix the chip to its bottom. After determining the reference positions, the axis system moves the tool to the height of the carrier substrate with a remaining distance of a few micron between the chip and the placed stack. Prior to the bonding process, the chip had been prepared with solder depots of 80µm size via solder jetting. In analogy to the LAB process described in section III the chip is vertically bonded to the side of the chip stack. During the bonding, the laser hits the chip's surface at an incident angle of 45°. The result of the initial bonding tests is displayed in Figure 16 and 17.

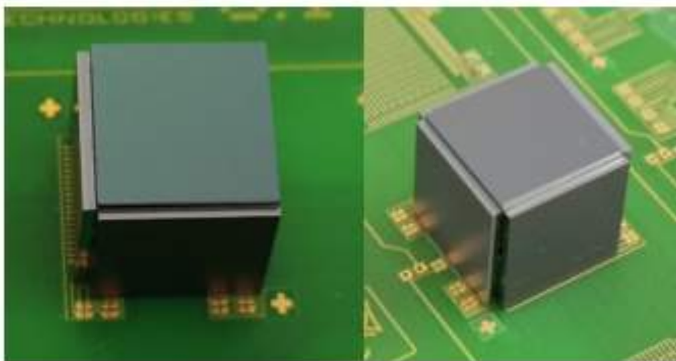

Figure 16: Chip stack with vertically bonded components at each side with dimensions of 12mm x 12mm x 12mm

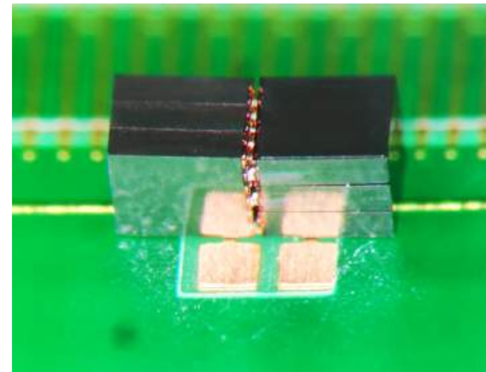

Figure 17: "3.5D" MEMS stack with dimensions of 0.9mm x 0.9mm x 0.9mm.

VI. Summary & Outlook

In this work, the TCB and LAB processes have been compared to each other regarding their properties and functionalities. It was found, that they significantly differ in important process parameters such as the thermal heat gradient over time and the overall process duration. In all aspects investigated, the performance, flexibility and speed of the LAB process either matched or surpassed that of the TCB process. Regarding the formation of the IMC layers and their resilience against aging as well as the avoidance of internal stress in a chip stack, the LAB process produced significantly better results than the TCB process. Nevertheless, the TCB process may require further process parameter optimization to insure proper IMC formation.

The concept of "3.5D" stacking was introduced, outlined and explained. It allows for vertical chip bonding, a technique, with which a microelectronic component can be vertically bonded to the side of an existing chip stack. All four sides of a chip stack can be contacted to generate a 3.5D package. This vertical chip bonding can not be achieved through the traditional TCB bonding process. It can, however, be performed using the LAB process described in this work.

In the future, "3.5D" stacking will make it possible to contact the individual layers in a chip stack via vertically bonded components and greatly reduce, if not eliminate the need for TSVs. This allows for taller stacks with more functionality, as conventional stacks need to reserve chip space in the lower layers for TSVs to contact the upper layers. Further, the persisting problem of heat dissipation is addressed, as the current bearing and therefore heat producing contacts are moved to the edges of the stack, where they can be cooled more easily. Finally, as chip designers embrace the possibilities of this new tool of manufacturing, completely new designs will become possible.

VII. References

[1] Santosh Kumar. *3D-IC and 2.5D TSV Interconnect for Advanced Packaging: 2016 Business Update* (Sep. 2016) Yole Development.

[2] Thorsten Teutsch et al. *LAPLACE-A New Assembly Method using Laser Heating for Ultra Fine Pitch Devices* (Jan. 2003) researchgate.net.

[3] Thomas Oppert. *Flip Chip Processes – Electroless UBM, Wafer Level Solder Sphere Transfer, Laser Solder Jetting & Laser Chip Bonding* (Nov. 2018) IMAPS UK Die Attach Workshop.

[4] Thomas Oppert. *Implementing laser heating for next generation packaging mass productions and beyond* (Sep. 2017) 1Executive Forum on Laser Technologies.

[5] Peter Kojo Bernasko. *Study of Intermetallic Compound Layer Formation, Growth and Evaluation of Shear Strength of Lead-Free Solder Joints* (2012) University of Greenwich. pp.31-32.

[6] Beáta Šimeková et al. *Growth of the IMC at the interface of SnAgCuBi (Bi = 0,5; 1,0) solder joints with Cu substrate* (2012) Tehnicki Vjesnik. nr.19, pp.107-110.

[7] Daniel Lu et al. *Materials for Advanced Packaging* (2009) Springer Nature.

[8] V. Jadhav et al. *Flip chip assembly challenges using high density, thin core carriers* (2005) Proc. 55th Electronic Components and Technology Conference. pp.314,319.

[9] Jie Li Aw et al. *Development of bonding process for high density fine pitch micro bump interconnections with wafer level underfill for 3D applications* (2013) Proc 63th Electronics Packaging Technology Conference. pp.543-548.

[10] T. Colosimo et al. *High Productivity Thermal-Compression Flip Chip Bonding* (Oct. 2014) In Proc. International Microelectronics Assembly and Packaging Society. pp.100-106