SMTA Press Release

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Wafer-Level Packaging Symposium (WLPS) Program Announced and Registration Now Open

Minneapolis, MN – The SMTA is pleased to announce the technical program for the Wafer-Level Packaging Symposium (WLPS). The symposium will be held February 15-17, 2022 at the DoubleTree by Hilton Hotel in San Jose, California.

The technical sessions on Tuesday and Wednesday are organized into three tracks: Wafer-Level Packaging (WLP), 3D Packaging, and Advanced Manufacturing and Test (AMT). The WLP track features sessions on materials, reliability, metrology, processing, and new technology, such as Fan-Out WLP. The 3D Packaging track features sessions on design, test, characterization, wafer bonding, chip stacking, and processing for fan-out. The AMT track features sessions on process materials, equipment, inspection, and more.

Packaging technology experts Joe Dickson, WUS PCB Ltd; Tanja Braun, Ph.D., and Michael Topper, Fraunhofer IZM; John Lau, Ph.D., Unimicron; and Jeff Gotro, Ph.D., InnoCentrix, LLC, are scheduled to lead half-day Professional Development Courses on February 17, 2022.

Registration for WLPS is now available online. Discounted rates are available for conference registration made on or before January 25, 2022. Visit https://smta.org/wafer for more information. If there are any questions, please call +1-952-920-7682 or email wafer@smta.org.

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SMTA is an international network of professionals who build skills, share practical experience and develop solutions in Electronics Manufacturing (EM), including microsystems, emerging technologies, and related business operations.

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