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2020 IWLPC
17th International Wafer-Level Packaging Conference

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IWLPC Panel Addresses Future Advanced Packaging Challenges

San Jose, California – USA – The International Wafer-Level Packaging Conference and Expo announces a panel discussion titled “Meeting Future Advanced Packaging Challenges: What's Next?” The live discussion will commence on Wednesday, October 14, 2020 at 9:00am US Pacific Time.

The panel will discuss challenges and possible solutions to advancements in heterogeneous integration, high density substrates, and Fan-Out Wafer-Level Packaging (FO-WLP) as they impact material selection, design and fabrication of features, inspection, test, and reliability. Attendees will be able to submit questions and get responses in real-time from the expert panel.

Panelists include Tim Olson, DECA; Tanja Braun, Ph.D., Fraunhofer IZM; Rahul Manepalli, Ph.D., Intel Corporation; Max Min, Ph.D., Samsung Foundry; and Shin-Puu Jeng, Ph.D., TSMC. The panel is moderated by E. Jan Vardaman, TechSearch International, Inc.

The panel discussion is open to all registered attendees. The technical conference and expo are available on-demand from October 13-30 with a live, online exposition enabled October 13 and 14. Details are available at the website: https://www.iwlpc.com/

For questions about the IWLPC conference, please contact Jaclyn Sarandrea, jaclyn@smta.org. For questions about the IWLPC expo, sponsorship, or advertising, please contact McKenna Hill, mckenna@smta.org or +1-952-920-7682.

About IWLPC

IWLPC brings together the semiconductor industry's most respected authorities addressing all aspects of wafer-level, 3D, TSV and integrated system packaging.

Going into its 17th year, the IWLPC is co-produced by *Chip Scale Review,* the leading international magazine addressing the semiconductor packaging industry, and SMTA, the distinguished global association representing electronic assembly and manufacturing professionals.

For more information visit: www.iwlpc.com