For more info contact:
Jaclyn Sarandrea
+1-952-920-7682
iwlpc@iwlpc.com

For immediate release – September 1, 2020

Samsung VP to Keynote IWLPC

San Jose, California – USA – The International Wafer-Level Packaging Conference and Expo announces Dan Oh, Ph.D., Engineering VP of the Test & System Package (TSP) unit at Samsung Electronics will deliver the opening keynote presentation of the virtual event. The presentation, "Trends, Challenges, Opportunities in Advanced Packaging for Smart Computing Era" will be released on Tuesday, October 13, 2020 at 9:00am US Pacific Time.

SAMSUNG

Dr. Oh is responsible for developing signal and power integrity and thermal solutions for memory, S. LSI and foundry devices. From 2016 to the end of 2019, Dr. Oh led the Package Development department responsible for both research and development of the entire Samsung product line. During this time, he helped establish an advanced wafer-level packaging laboratory for developing high-end server products such as 2.5D Silicon/RDL interposers, FO-WLP and 3D TSV devices. He also helped research and grow FO-PLP technology for consumer and mobile products commercializing the world's first FO-PLP product for the Galaxy watch. Dr. Oh received his Ph.D. in electrical engineering from the University of Illinois, Urbana-Champaign in 1995. He has over 30 years of experience in the packaging and signal and power integrity fields with multiple high-tech companies, including Intel, Rambus, and Synopsis. His dedication to his work has led to over 90 patents, patent applications, and over 160 published papers in IEEE journals and conferences. He is also the lead author of the book "High-speed Signaling: Jitter Modeling Analysis and Budgeting."

The keynote presentation is open to all registered attendees. The technical conference and expo are available on-demand from October 13-30 with a live, online exposition enabled October 13 and 14.

For questions about the IWLPC conference, please contact Jaclyn Sarandrea, jaclyn@smta.org. For questions about the IWLPC expo, sponsorship, or advertising, please contact McKenna Hill, mckenna@smta.org or +1-952-920-7682.

About IWLPC

IWLPC brings together the semiconductor industry's most respected authorities addressing all aspects of wafer-level, 3D, TSV and integrated system packaging.

Going into its 17th year, the IWLPC is co-produced by *Chip Scale Review,* the leading international magazine addressing the semiconductor packaging industry, and SMTA, the distinguished global association representing electronic assembly and manufacturing professionals.

For more information visit: www.iwlpc.com