



International Wafer-Level Packaging Conference Press Release

For more info contact:

Jenny Ng
952-920-7682
iwlpc@iwlpc.com

For immediate release – August 29, 2017

International Wafer-Level Packaging Conference (IWLPC) Workshops

Minneapolis, MN - The SMTA and *Chip Scale Review* are pleased to announce the Workshops for the 14th Annual International Wafer-Level Packaging Conference (IWLPC) held October 26th. IWLPC will be held October 24-26, 2017 at the DoubleTree Airport Hotel in San Jose, California.

Two workshops are scheduled for the morning of October 26th. John Hunt, ASE (US) Inc., will instruct “Fan-Out Packaging – Technology Overview and Evolution,” providing an overview of the drivers, technology, advantages and disadvantages of various structural and processing options, as well as a view of potential future trends for Fan-Out Packaging.

Concurrently, Fernando Roa, Ph.D., Amkor Technology, will lead the course “Package on Package, Design, Process and Quality,” delving into critical design rules to observe during the layout of the substrates required for such packaging as well as best known methods for assembly including rules of thumb for selection of materials, typical process flows, and quality metrics.

Two workshops are also slated for the afternoon. John Lau, Ph.D., ASM Pacific Technology, will discuss recent advances in fan-out wafer/panel level packaging, 3D IC packaging, 3D IC integration, 2.5D IC Integration, embedded 3D hybrid integration, 3D CIS/IC integration, 3D MEMS/IC integration, and Cu-Cu hybrid bonding in his workshop “Fan-Out Wafer-Level Packaging and 3D Packaging.”

That same afternoon, Rao R. Tummala, Ph.D., Georgia Institute of Technology, will instruct “Future of Packaging: Embedded and Non-embedded and Fan-Out.” The course will review the current approach to devices, device packaging and system packaging including traditional single- and multi-chip packaging as well as the recent focus in embedded and fan-out packaging.

Visit www.iwlpc.com for more information.

Contact Jenny Ng at 952-920-7682 or iwlpc@iwlpc.com with questions.

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