SMTA Press Release

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For immediate release – January 7, 2025

Wafer-Level Packaging Symposium Program Announced

Minneapolis, MN – The SMTA is excited to announce the technical program for the 2025 Wafer-Level Packaging Symposium. The symposium will be held February 18-20, 2025 at The Hyatt Regency San Francisco Airport in San Francisco, California.

The technical program features a special keynote presentation. On Wednesday, February 19, 2025, Eric Breckenfeld, Nvidia, and Erik Hadland, Semiconductor Industry Association, will co-present, “The CHIPS and Science Act: Past, Present and Future of U.S. Microelectronics R&D.” For more information, click here.

Technical sessions include over 20 expert speakers who delve into wafer-level packaging advances, assembly/integration process, novel interconnect & packaging process and materials, substrate/integration platform, test & metrology, fan-out wafer-level packaging, and more. The program features presentations from leading companies including adeia, Nvidia, NHanced Semiconductors, Semiconductor Industry Association, and universities such as Hanyang University, Yokohama National University, and more. View the full technical program here.

The symposium kicks off with two professional development courses on Tuesday, February 18, 2025. The first course, “Materials for Semiconductor Packaging,” will be instructed by Terry Alford, Arizona State University. Gamal Refai Ahmed, Ph.D., AMD, will instruct the second course, “Current & Future Challenges and Solutions in AI & HPC System & Thermal Management.” Access to these courses is included in standard registration. For more information, click here.

Registration for this event is open. Click here to register. Discounted rates are available by registering on or before January 27, 2025. All presentations, professional development courses and events open to attendees are included in registration.

For more information about the Wafer-Level Packaging Symposium, please contact Kristin Nafstad at kristin@smta.org or +1-952-920-7682.

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The SMTA membership is an international network of professionals who build skills, share practical experience and develop solutions in electronic assembly technologies, including microsystems, emerging technologies, and related business operations.

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