

Laser Assisted Bonding (LAB) for Fine Pitch Cost Effective Interconnection

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I. Abstract

The adoption of fine pitch copper (Cu) Pillar bump has been growing as the solution for high performance and low-cost flip chip packages. Higher input/output (I/O) density and very fine pitch requirements are driving very small feature sizes such as small bump on a narrow pad or bond-on-lead (BOL) interconnection. At the same time, higher performance requirements are driving increased current densities, thus assembling such packages using a standard mass reflow (MR) process and maintaining its performance is a real and serious challenge. Thermal compression bonding (TCB) using non-conductive paste has been used to mitigate the assembly risk, up to a certain extent, of die size and package body size. On the other hand, the TCB process results in a significantly higher assembly cost due to very low throughput. The very cost sensitive semiconductor market is not ready to adopt the TCB process for this reason. To address the need for fine pitch Cu pillar bumps, a new method of attaching fine pitch bumps called laser assisted bonding (LAB) has been successfully introduced in flip chip packages. No additional reflow process or excessive compression force is required. It's a very localized process and requires only a few seconds to join the chips with the substrate. Due to the very quick process thermal budget and materials, thermal expansion mismatch is much lower than MR or TCB which results in less package warpage and less die level stress. However, the laser scanning length of LAB is still limited to a certain size. As a result, throughput is about half of MR, but compared to TCB, it is 2 to 3X higher.

II. Introduction

MR continues to be the mainstream process for flip chip packages, while TCB with non-conductive paste (NCP) used to be the best solution for finer bump pitch flip chip die [over the](#) last few years. TCB certainly provides better chip attach yields with higher alignment accuracy, however it is [a](#) very slow process and quite often the bump shape becomes an issue due to excessive bond force. Other issues are die crack, higher die/package warpage, etc. LAB is the most attractive alternative to overcome these issues. In this process, thermal energy from the IR (infra-red) laser heats up the die and makes the joint between the die and substrate using fine interconnection. A typical LAB schematic process is shown in Figure 1 below.

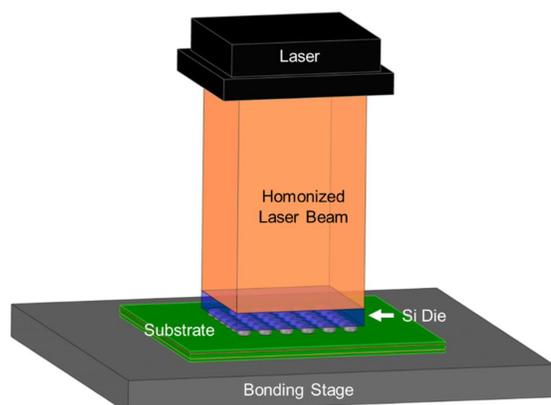


Figure 1: LAB Chip Bonding Process (Courtesy: link.springer.com)

III. Interconnection Process Evolution

There are various advantages of the LAB process over conventional mass reflow such as [the](#) very quick chip joining process (only few seconds), no additional reflow process,

higher yield, less die stress, warpage, capability to use a much wider process margin, etc. [Historical-The historical](#) evolution of LAB from MR is described in Figure 2 below.

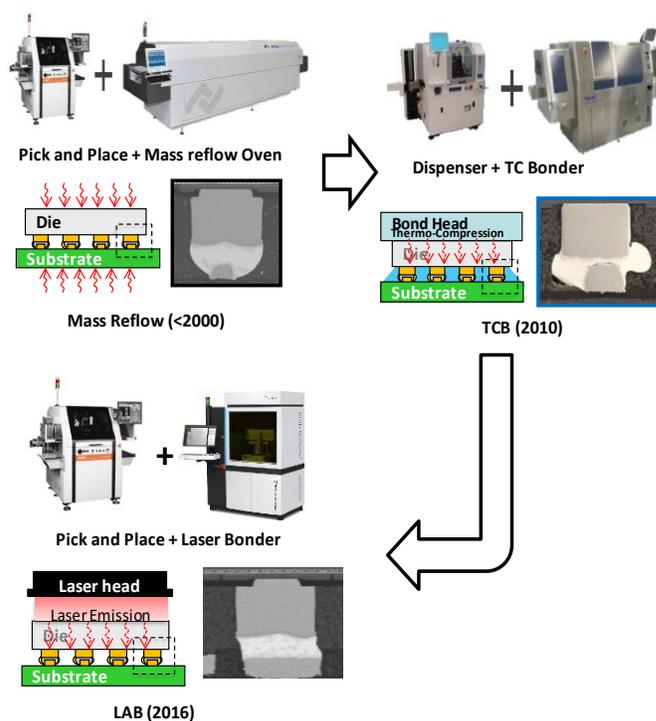


Figure 2: Evolution of various chip joining technologies from traditional mass reflow (MR) to thermal compression bonding (TCB) to latest laser assisted bonding (LAB) for advanced flip chip technology

Thermo-mechanical results found approximately 60% lower die stress with the LAB process than MR as shown in Figure 3.

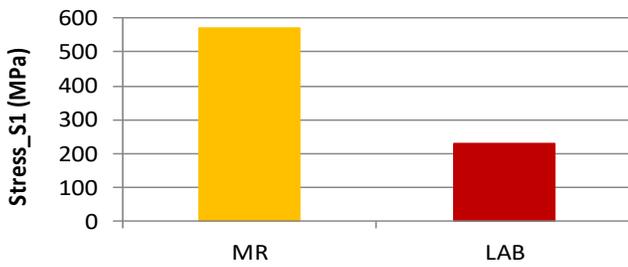


Figure 3: Die stress simulation result between MR and LAB

IV. Process Characterization DOE and Results

Numerous studies have been conducted on actual packages since early 2016 to make sure LAB data provides substantial benefit over standard MR and TCB before ramping into mass production. In terms of the assembly process, there is no difference between MR and LAB except that the MR reflow process is interchanged with LAB. Both CUF and molded underfill (MUF) can be used in the LAB process. LAB process substrates don't need to be heated at a very high temperature like MR, therefore, it only takes only a few seconds to heat up the die and perform chip joining.

Very clear crack or rupture was observed in the die ELK layer for the MR leg, whereas no visible crack was found with the LAB leg as shown in Figure 4 and 5 for fcFBGA and fcBGA data respectively.

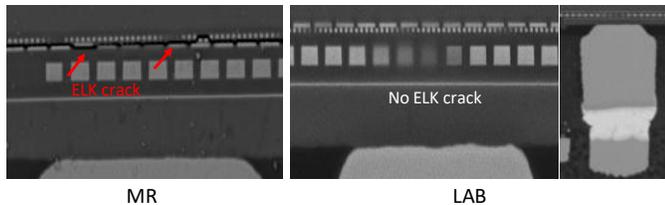


Figure 4: Die ELK crack data after QTC 20X. No ELK crack with LAB upto 60X QTC

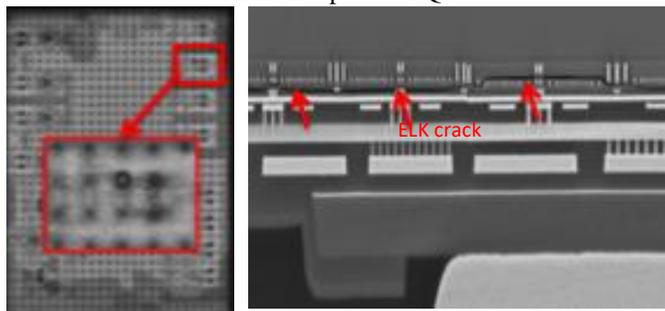


Figure 5: fcBGA ELK crack after 10X QTC with MR

Extensive long-term package level reliability tests with the LAB chip attach process were successfully completed for fcFBGA and fcBGA packages. This technology is currently in mass production for fine pitch and small UBM packages. Based on the reliability data, no noticeable concerns have been raised so far. After reliability tests, some of the packages were sliced to make sure no anomaly were present in the die, ELK

layer bump or substrate layers. Figure 6 shows some of the cross-section data after package level reliability tests. LAB has been used to attach DDR CSP and other passive components with the SOC package without any performance degradation of the SOC die. Recently, DRAM packages were attached with baseband or application processor die in a package on package (PoP) structure. With the help of LAB, package pre-stacking can be done very smoothly at much higher yields. Pre-stacking packages with LAB are already qualified for mass production. Extensive package characterization data found that solder joint integrity looks much better than traditional MR. Figure 7 shows some cross-section pictures of a PoP where LAB was used for top and bottom package attachment. This process has been widely used for mobile and consumer package attachment.

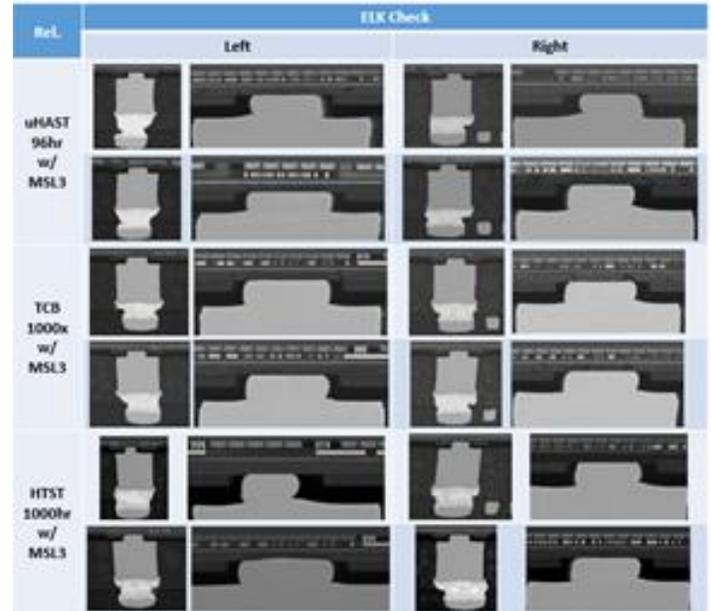


Figure 6: SEM cross-section of the packages after long term reliability tests

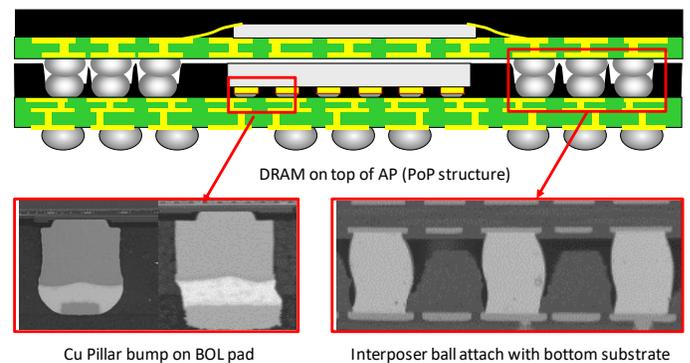


Figure 7: LAB use to attach DRAM with AP. Cross-section data shows very good solder joints

V. References

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