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INTELLIGENT INSPECTION

Essential Inspection Requirements in the Era of Convergence

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In the fast-paced world of electronics manufacturing, the convergence between semiconductor packaging and surface mount technology (SMT) has revolutionized the industry. This merging of technologies has led to the development of innovative, automated optical assembly machines and advanced software that play a pivotal role in ensuring the quality and reliability of electronic devices. To achieve optimal results, it is crucial to understand and address the essential inspection requirements specific to these advanced solutions to help manufacturers optimize their processes, reduce errors, and enhance the overall production quality.

The Challenges

Revered Intel co-founder Gordon Moore coined "Moore's Law" in 1975, which predicted that transistor density in semiconductor integrated circuits would double every two years. Until about the 2020s, this law was undisputed, but the necessary manufacturing processes are nearing their limits and economics are becoming an issue. The cost of designing a semiconductor on a 5nm process is $540M, which is about twenty times the cost of a 65nm chip and nearly double the cost of its immediate predecessor, a 7nm semiconductor. What's more, the cost of building a semiconductor fab is also staggeringly different from 65nm, which can cost more than twice as much as a 7nm fab (Figure 1). This cost increase could be acceptable if the price of the product could increase accordingly, however, the price of semiconductors does not simply increase in direct proportion to the increase in density. Rather, prices fluctuate depending on economic factors like supply and demand, so companies can no longer bet on unconditional density improvement.

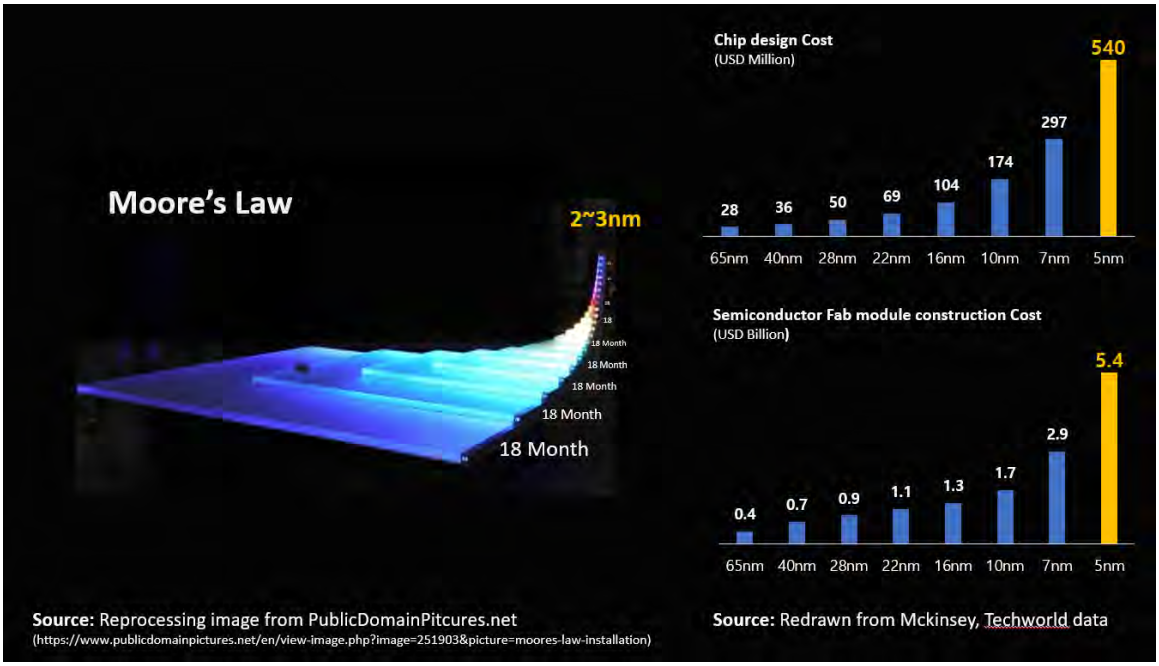

Figure 1: Moore's Law as Applied to Chip Design and Wafer Fab Construction Costs

Currently, bleeding-edge manufacturing processes are at 2-3nm, which is too fine to produce chips at commercially viable yield levels using existing materials and processes. In addition, the cost savings that come with increased density have reached their limits. Therefore, many companies are looking for alternatives to solve this problem. Of course, there is the development of core material technologies, but many companies are now focusing on packaging technologies to improve the performance of semiconductor products. For example, EMIB (Embedded Multi-Die Interconnect Bridge), Chiplet, FOWLP, Stacking, SiP, and more. Advanced packaging technologies with heterogeneous integration is inevitable and extremely important (Figure 2).

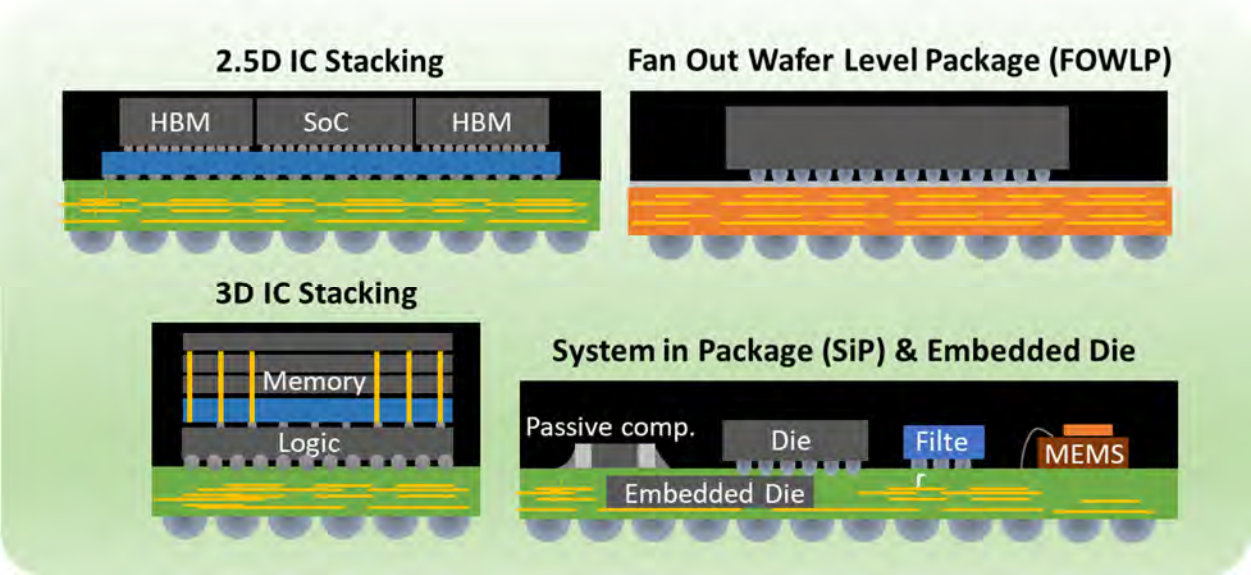

Figure 2: Examples of Packaging Technologies Designed to Improve Processing Performance

Process Evolution

The areas of PCB assembly and package assembly were different when it comes to chronology, but there is a big shake-up in technology underway. Due to Moore's Law limitations, alternative packaging technologies are gaining attention. So, research to improve the process has affected both fields being necessary.

The need for different, thinner, and denser technologies has challenged the manufacturing processes in these two areas. In semiconductor packaging, we are seeing a move toward packaging on the wafer itself, which is driving a wide range of attempts. In the PCB area, there is a demand for thin and dense mounting technology at the level of semiconductor packaging. In this process, there is an intersection between the two fields that is creating heterogeneous packages in an overlapping area (Figure 3).

In this area, we need to overcome complex applications, e.g., the inspection of various SiP products including RF modules and die inspection on Substrate-like PCBs (SLPs). Also, specific to the semiconductor packaging manufacturing process, manufacturers widely adopt SMT processes in Wafer Level SiP and Embedded PCB as well. Clearly, the two industries are now converging.

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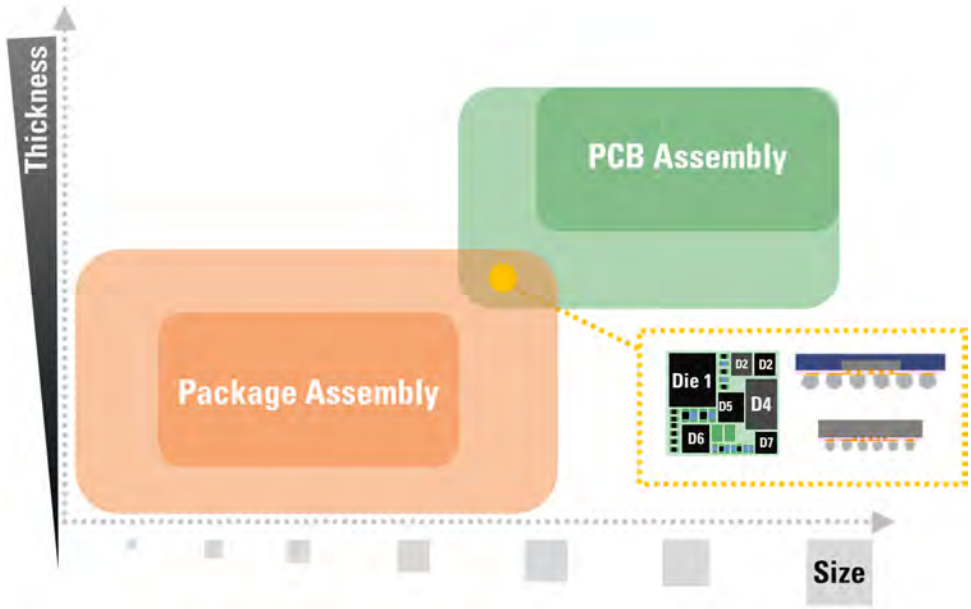

Figure 3: Overlapping Package and PCB Assembly Technologies Creating Heterogenous Packages

Converging Processes

Given these trends, what are some of the equipment requirements that you should consider when choosing your inspection equipment? For example, if using the existing semiconductor packaging inspection solutions to cover this overlapping area, the performance of the system itself may not be an issue, but it may have a cost-performance issue. Meanwhile, SMT inspection equipment may have some performance issues for fine-pitch small and shiny component inspection, which we are expecting as bottlenecks on this overlapping area.

Before we decide the optimized inspection solution for those areas, though, consider the approximate flow from the package assembly process, which is from the back-end semiconductor process to the PCB assembly process. Basically, SiP or System in Package belongs to the semiconductor package process, but it can also be seen as a high-end SMT process such as SLP, if considering that various components including die are mounted on the substrate PCB (Figure 4). If we look at it this way, we can conclude that the boundaries between the semiconductor package process and the SMT process are blurring or converging in the hybrid or heterogeneous SMT area. Manufacturers need an inspection system that can support both industries.

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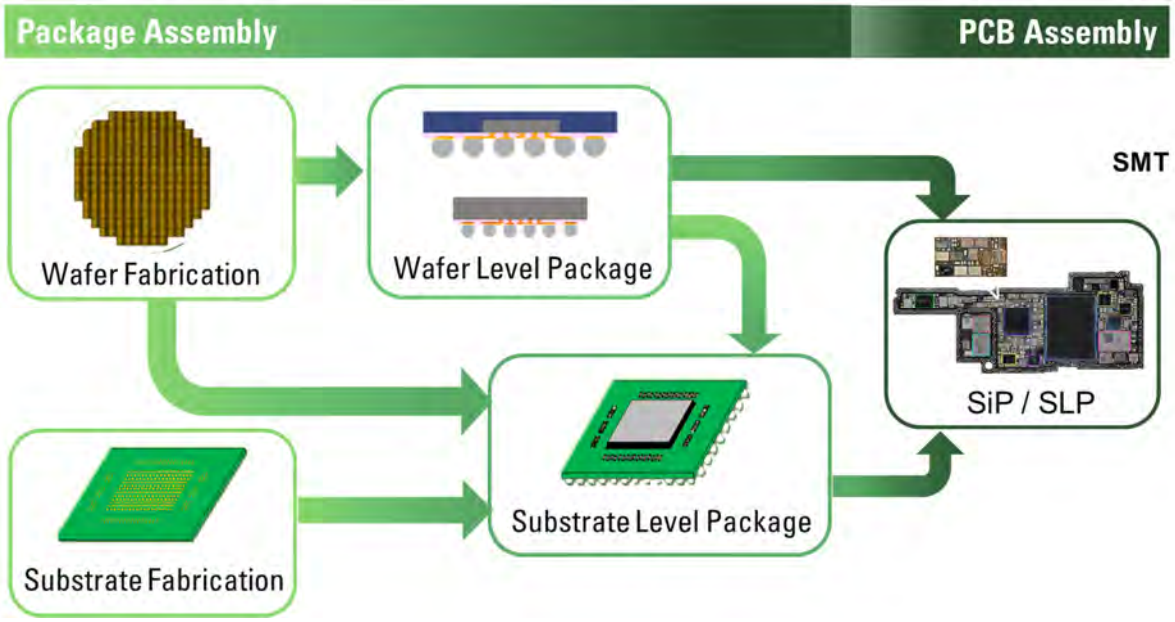

Figure 4: Blurring Process Flow from Wafer to PCB Assembly

In this era of technology convergence, let us consider inspection requirements for both industries, based on the flip-chip BGA (FCBGA) package and chip mounted high-end board. The common inspection requirements for both industries are grouped into three categories. First, the inspection of the die and passive components. This is simply the area where an automated optical inspection machine (AOI) inspects packages and components. Next is inspection after dispensing, such as flux inspection, die C4 area underfill, or BGA ball side underfill. Finally, soldering inspection. For example, solder bumps in the C4 area, package ball inspection such as FCBGA, flip-chip chip scale package (FCCSP), wafer-level chip scale package (WLCSP), and printed solder paste inspection on general PCB or wafer. The era of convergence is here (Figure 5).

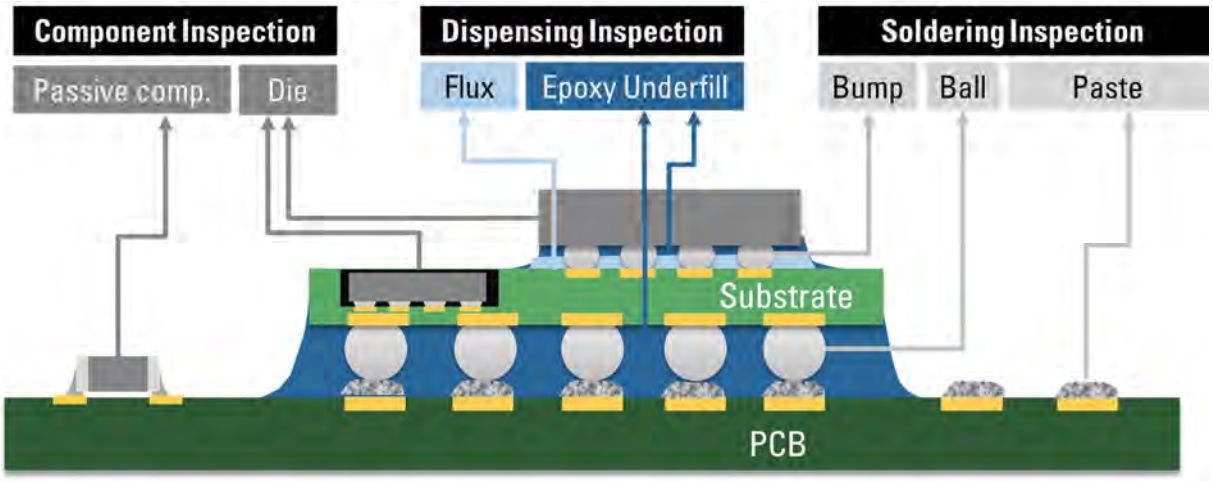

Figure 4: Examples of Converging Technologies Requiring Similar Inspection Requirements

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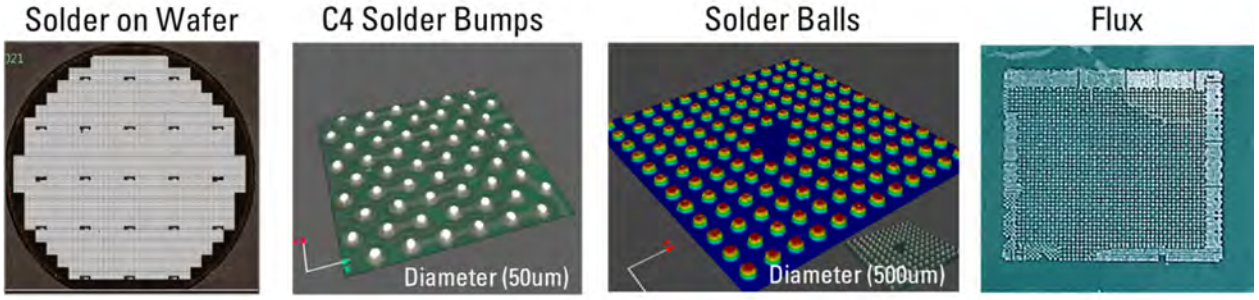
Inspection Solutions

In response to these different inspection needs in advanced packaging and high-end SMT, Koh Young has developed four unique inspection systems to address specific processes and applications with industry awarded innovative technology. In fact, with the emergence of many different packaging technologies, there will be a variety of processes in the market, not just a single process.

Solder & Flux Inspection

First, there is a need for printed solder deposits, bumps, BGA ball inspection, and flux inspection. Needs for those applications span semiconductor packaging to substrate fabrication processes, and then covering all the way up to high-end SMT processes.



Introducing the Meister S, a premium in-line 3D inspection system for micro-sized, thin solder paste:

- 3.5um resolution, 25 mega-pixel, high-speed camera suitable for volume production
- 30um diameter bumps inspection with 0.1um Z resolution
- Optimized image processing and advanced algorithms for upwards of two million bumps
- Z-tracking technology and pad referencing for spatial geometry distortion correction and warpage compensation
- Transparent flux inspection with proprietary optical configuration and algorithms

To give a better frame, C4 solder bump and 0201M solder deposits are exceedingly small. In the case of C4 bump, the surface is very shiny, making it difficult to get a stable 3D measurement. With the Meister's 3.5um resolution, 25 mega-pixel high-speed camera, and AI-based inspection algorithms, it effectively measures and inspects C4 bumps and 0201M micro solder deposits. In the case of BGA solder balls, the diameter is much larger than C4 bumps, but are also shiny, so inspection with traditional tools is a challenge. However, the Koh Young Meister S reliably produces 3D measurement results. Additionally, as the size of solder bumps becomes smaller and denser, some processes will dispense flux instead of bumping in the C4 area. Regardless, the Meister S can help manufacturers control the quality of the flux dispensing process to ensure high yields and low defects.

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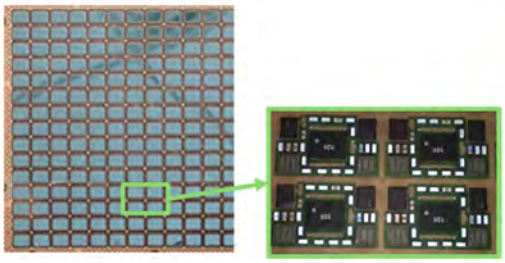
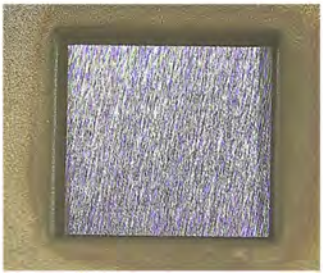
Die & Component Inspection

Next, it is about die and component placement. This requires reliable inspection performance for 0201M-sized components with very narrow pitches that also includes inspecting die with mirror-like surfaces. In some cases, it is also necessary to have an inspection capability for embedded die mounted inside a cavity on the substrate.

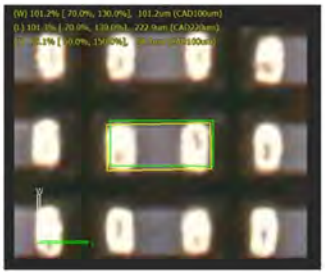
System in Package (SiP) Die



Embedded Die



0201M (008004 EIA) Chip



Introducing Koh Young's Meister D and Meister D+ solution for SMT component and semiconductor die inspection. Suitable for inspection of high-density placement and shiny die, the Meister D series has the following key features:

- Small Die and Component Inspection (0201 Metric / 008004 EIA)
- Superior Inspection Performance, powered by A.I. developed by Koh Young Research America
- Full 3D Height and Tilt Measurement for High Density Placements down to 50um gap
- Robust Inspection for Die, Component, and LED devices

Let us consider the two processes. First, component SMT inspection. The Meister D series provides multiple projection technologies to solve the shadow problem and deliver stable 3D inspection results. It can handle high-density placements with only a 50um gap or chip components mounted between taller BGA packages, which can cause shadow problems and interfere with traditional inspection approaches.

Next is a solution for highly reflective die surfaces that makes 3D inspection virtually impossible because of optical triangulation issues. To solve this issue, Koh Young developed a unique optical solution for measuring the die. By applying this new 3D measurement technology, it is possible to reliably inspect die in 3D – even die with mirror-like specular reflection. It even inspects embedded die in a cavity without any issues.

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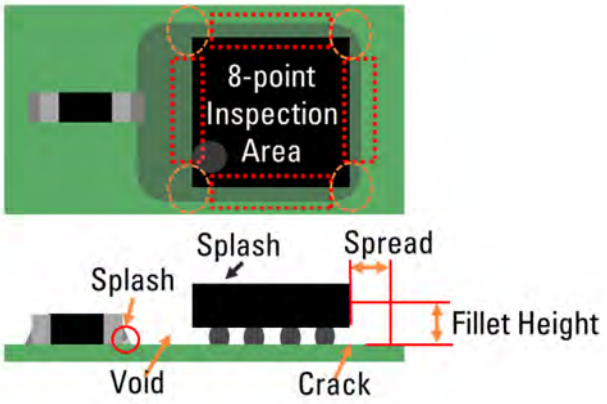
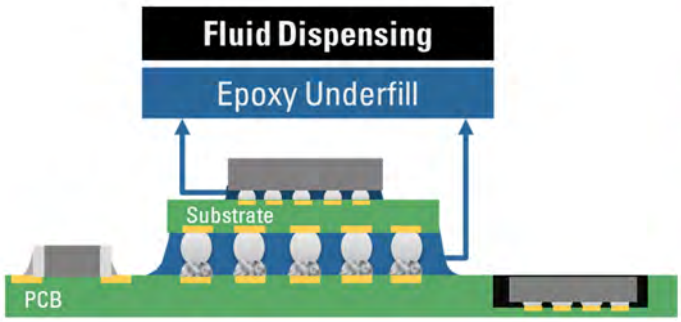
Underfill Inspection

Following die placement, some manufacturers apply an epoxy underfill to improve the die attach process or ensure BGA joint reliability. Therefore, they have a need to inspect the underfill thickness to ensure proper application and formation; however, it is a challenge to detect the 3D cross-sectional thickness of the liquid underfill.



The award-winning Koh Young Neptune C+ is a breakthrough in 3D measurement for dispensing inspection. It is capable of measuring thickness profiles for transparent liquid applications such as epoxy underfill and conformal coatings. Neptune C+ has the following features:

- True 3D profiling measurements across the entire area at production speed
- L.I.F.T. technology (Laser Interferometry for Fluid Tomography) delivers non-destructive 3D inspection to precisely measure fluids – wet or dry
- Simple, Intuitive Programming and User Interface
- Machine-Learning algorithm and AI helps the Neptune accurately measure for coverage, thickness, and consistency



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Wafer Level Inspection

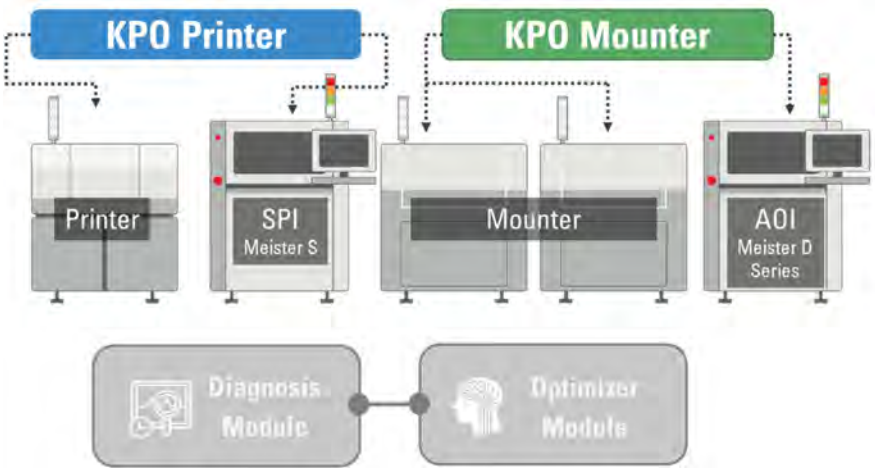
Today's electronic devices are becoming more complex with increased functionality and higher performance; yet the packages are shrinking and require higher placement density. Wafer-Level Packaging (WLP), the technology of packaging a die while still on the wafer, is considered the next generation packaging technology. Not only does WLP maximize production yield, but it also reduces manufacturing costs. Companies can further maximize yield without increasing costs by detecting defects at the wafer stage with accurate inspection.

WFP requires a solution that can use wafers or ring frames, and Koh Young developed the Meister W series for these wafer level processes. It combines innovative vision algorithms and high-resolution optical technologies to inspect wafer bumps, pillars, and highly reflective die, as well as SMT components. Using the mainstay of semiconductor automation, we integrated a dual-arm Equipment Front End Module (EFEM) to handle wafers and ring frames in touchless cleanroom environment. The Meister W series offers the following features:

- Proprietary deep learning technology for enhanced inspection of cracks, FOD, chipping, and more
- Industry-leading True 3D measurement capabilities enhanced by proprietary deep learning technology
- 10-micron diameter wafer bump inspection
- True 3D height and tilt measurement on shiny die
- Integrated 300mm EFEM
  (Equipment Front End Module)

AI-powered Process Improvement

Yield improvement goes beyond inspection machine performance. At Koh Young, it is our award-winning KPO (Koh Young Process Optimizer) software suite. In the case of solder paste inspection (SPI), we use KPO Printer to communicate directly with the printer and adjust the pressure, speed, and separation speed in real-time to improve the print quality. In addition, KPO Mounter will communicate directly with the mounter to analyze which pad or nozzle has a problem. If it is not a pad or nozzle problem, but a programming tuning problem, we have a solution to fix it by a mounting position adjustment. KPO is an innovative machine learning modeling technology that analyzes data to determine the factors contributing to a failure, and then corrects them with automated feedback and optimized settings.



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The Era of Convergence

In the era of convergence between semiconductor packaging and SMT manufacturing, automated optical assembly machines and software play a pivotal role in ensuring the quality and reliability of electronic devices. Precise die and component inspection, reliable solder joint and bump or ball inspection, and the capabilities of AI-powered optical inspection software are essential requirements for these machines. The integration of automated optical assembly machines and software with manufacturing systems enhances overall operational efficiency, facilitates real-time monitoring, and provides valuable insights for continuous improvement.

As the industry continues to evolve, manufacturers should embrace technological advancements, such as AI, machine learning, and big data analytics, to further enhance inspection processes and optimize SMT, advanced packaging and semiconductor production operations. By meeting the essential inspection requirements and embracing future advancements, manufacturers can produce high-quality devices that meet the demands of the modern market while staying at the forefront of the manufacturing industry.

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