

# Press Release: Corporate News/Events

For Immediate Release

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## **ZESTRON to Present "Optimizing High Bandwidth Memory (HBM) Wafer Surface Treatment: Navigating Cleaning Challenges" at SMTA Wafer Level Packaging Symposium**

**Manassas, VA** – February 5th, 2023, ZESTRON, the leading global provider of high-precision cleaning products, services, and training solutions in the electronics manufacturing and semiconductor industries, proudly announces that Senior Application Engineer Ravi Parthasarathy will be presenting a technical session titled "Optimizing High Bandwidth Memory (HBM) Wafer Surface Treatment: Navigating Cleaning Challenges" at the upcoming Surface Mount Technology Association (SMTA) Wafer Level Packaging Symposium.

Scheduled for February 13th, 11:30 AM to 12:00 PM, Ravi Parthasarathy's presentation will delve into the intricacies of enhancing High Bandwidth Memory (HBM) wafer surface treatment processes while addressing the unique cleaning challenges associated with this advanced technology.

As a seasoned professional in the electronics manufacturing industry, Ravi brings a wealth of knowledge and hands-on experience to this presentation. His insights into optimizing HBM wafer surface treatment will prove invaluable for engineers, researchers, and professionals seeking to stay at the forefront of wafer-level packaging advancements.

For more information about the SMTA Wafer Level Packaging Symposium and to attend Ravi Parthasarathy's presentation, please visit <https://smta.org/BlankCustom.asp?page=wafer>.

**About ZESTRON:**

ZESTRON is headquartered in Manassas, Virginia, and operates in more than 35 countries. With eight technical centers worldwide and the industry's most knowledgeable team of engineers focused on high-precision cleaning, ZESTRON's commitment to ensuring that its customers surpass even the most stringent cleaning requirements is without equal.

For additional information or to tour one of our technical centers, please visit [www.zestron.com](http://www.zestron.com).

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