Backside Metallization for Low Cost High Thermal Package

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Abstract
Advanced semiconductor packaging requirements for higher and faster performance in a thinner and smaller form factor with significantly higher thermal dissipation continue to be the driver for mining and artificial intelligence (AI)/high performance computing (HPC) applications. While the increase in device performance or input/output (I/O) density is driven by the famous "Moore's Law," the packaging industry is experiencing opposing trends for more complex packaging solutions with the expected cost targets moving downward.

Packaging technology has become more challenging and complicated than ever before driven by advanced silicon (Si) nodes, finer bump pitches, as well as finer line width and spacing substrate manufacturing capabilities to satisfy the increasing requirements in the semiconductor industry. As increasing I/O counts and high thermal performance are needed in computing, and AI/HPC devices, packaging solutions are migrating from traditional, QFN or FLGA to flip chip CSP (fcCSP) and high end flip chip BGA (fcBGA) with a metallic lid to dissipate heat. For very high pin count AI/HPC, the solution will eventually go to 2.5D with memory integration where packaging cost is not the primary concern. For low to medium end computing applications, removing the heat from the die backside without adding much packaging cost is a major challenge.

Typical thermal die power for low to medium end thin flip chip CSP packages is a few watts. There are various ways to mitigate the thermal concern for fcCSP packages such as exposing the die backside, high conductive mold compound, adding a metal lid to the die backside, thicker metal layers in the substrate, die backside metallization, etc. Adding extra packaging cost for small to medium thermal improvement cannot be justified for a cost sensitive market.

In this study various ways of improving thermal performance of a fcCSP package are investigated and die backside metallization was finally selected as the optimum solution for low to medium die power packages. A thorough thermal simulation DOE was conducted to justify the backside metallization concept. This backside metallization process has been integrated into high volume assembly line. Various material and processes are considered to successfully qualify the package. The detailed assembly process along with mechanical reliability data are published in the paper.

Keywords: flip chip, backside metallization, thermal performance, mining, artificial intelligence, high performance computing, fcCSP.

I. Introduction

The computing market is one of the highest growth industries and it continues to strive by making faster semiconductor chips and procuring massive land for data facilities across the globe. Recent economic data show that the mining, artificial intelligence (AI), and high performance computing (HPC) economy is flourishing at a good rate and this type of venture has become quite profitable for many mining operations, and chip manufacturers.

Fine pitch Cu pillar bumps are widely used for high performance packages. Certainly fine pitch bumps encountered some assembly challenges in chip attach process. Various ways of chip attach processes have been introduced in the assembly line to overcome challenges for next generation higher hash power mining with advance Si nodes (≤14nm or 7nm). Effective way of managing thermal dissipation is another major challenge for high power computing chips. Some of the small chips are introduced with 5 to 10W of die power. Selecting the right BOM (bill of materials) and process is a key to qualify high thermal chips for AI/HPC. Various material and processes have been taken into consideration in the industry to successfully qualify the packages used for high power applications. As chip technology gets more and more advanced along with the aim toward product miniaturization, the need to reduce the chip package form factor while increasing chip performance has become critical to enabling more advanced chip technology and product miniaturization. Flip chip is the best high density and reliable interconnection technology for fine pitch or ultra-fine pitch (<40um pitch) applications. In today's market the main driver for fine pitch flip chip is mobile and some consumer applications. As demand for increasing input/output (I/O) counts in mobile devices grow, packaging solutions are migrating from traditional wire bond packages to fine pitch flip chip interconnect to meet these requirements.

Typically, high power flip chip packages include both a lid and heatsink to control heat from package to the ambient. Figure 1 shows the lid and heatsink attached flip chip package. Thermal interface materials (TIM) are used to remove heat from die to the ambient.

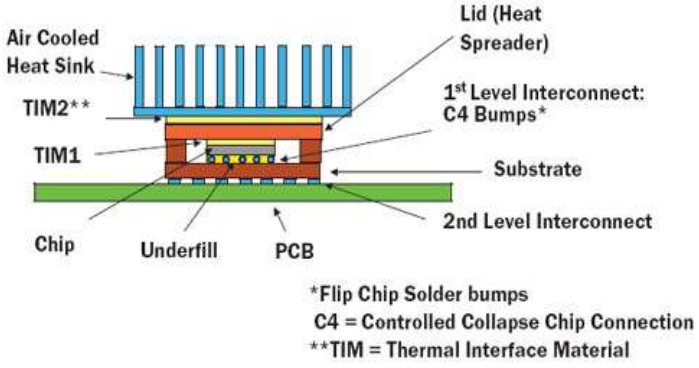

Figure 1: Typical high thermal flip chip package with lid and heatsink attached (courtesy: electronic cooling)

Package thermal performance depends on few important parameters such as thermal interface material type, lid type, substrate type and design, underfill/mold compound type, lid attach process, system conditions, etc.

II. Thin fcCSP for High Thermal Applications

In flip chip packaging technology, there are various solutions available to manage the die power of the device. Thinner fcCSPs are typically built with overmold compound, exposed die overmold, or bare die with underfill. Overmold packages enhance package rigidity and provide better mechanical life; however, overmold may not be a good choice for high power package. Various types of thin flip chip CSP (fcCSP) schematics are shown in Figure 2. Standard mold compound comes with very low thermal properties. Currently mold compound suppliers are adding higher thermally conductive fillers to increase thermal performance of molded flip chip packages. Adding conductive filler with higher filler content sometimes can be a big challenge due to higher viscosity, poor workability and higher cost. Moreover, high conductive mold compound is very limited in the market. Adding more thermal vias and using thicker Cu in the substrate enhances package thermal performance somewhat. Thicker power and ground planes not only improve thermal, but can also improve current carrying capabilities. Typical Cu planes in the substrates are with 1Oz, but recently 2Oz Cu planes have also been used for better thermal performance. A 4L substrate with thicker (2Oz) Cu planes is shown in Figure 3 below. In this case, heat from the chip is transmitted to the inner layers via the bump pad's through-holes, which also serve as grounds, and two out of the four inner layers are used as grounds to secure a heat dissipation path. In recent days coreless ETS (embedded trace substrate) or MIS (molded interconnect substrate) with thicker metal layers are widely used for high thermal and power fcCSPs.

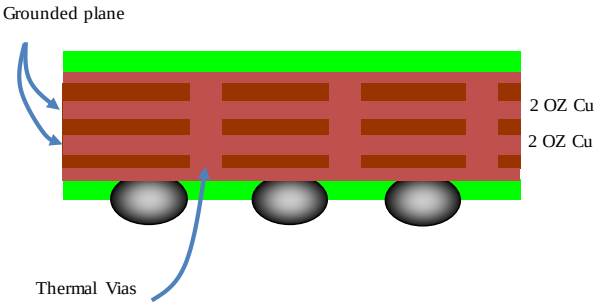

Figure 3: Thermal vias with thicker (2Oz) Cu in the laminate

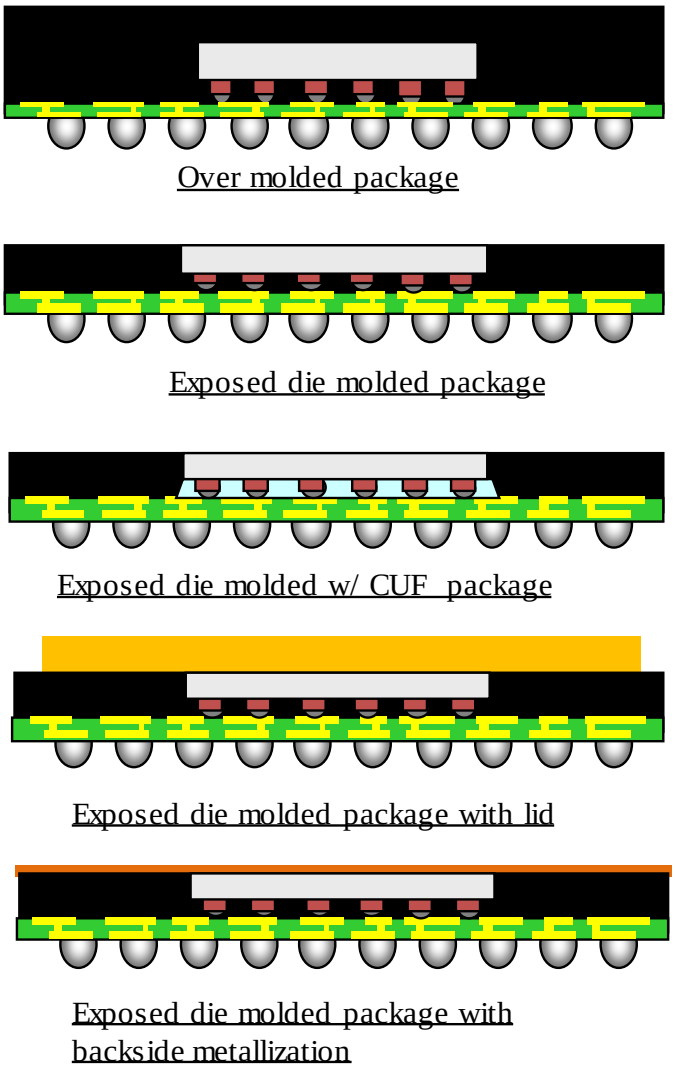

Figure 2: Various types of fcCSP

Only exposing the die backside without attaching a lid or system enclosure may not improve thermal performance. However, exposed die packages will always leave an option open to attach an enclosure of the system if needed. Exposed molded packages makes the package much thinner than an overmolded or lidded package, which makes the package a fit for applications where the Z height is very critical. Single die as well as multi dies along with some passives can be attached in one single fcCSP. A lid or heatspreader certainly improve thermal performance of the package irrespective of boundary conditions. Attaching a lid with the die backside increases spreading of heat flux over the package and hence, dramatically decreases thermal resistance. A simulation DOE has been conducted for molded and exposed die molded with lid packages to understand the effect of thermal resistance of the package. Figure 4 shows a lidded vs an exposed die molded package for multi die fcCSP. Standard vs high thermal conductivity EMC are also added in the simulation DOE. Table 1 shows that an exposed die lidded package has much lower thermal resistance than an overmolded package. Adding high thermal EMC also improves thermal resistance as shown in table 1 below.

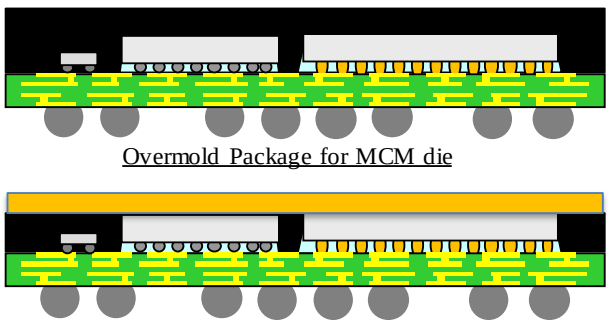

Figure 4: Thin fcCSP overmolded and lidded with MCM die

Classification		EMC	*Mold clearance	Q_{JC-max} (°C/W)
1	Overmold	0.9W/mK	0.18mm	5.88
2	Exposed + heat spreader	0.9W/mK	0	1.46
3	Overmold	3.0W/mK	0.18mm	2.29
4	Overmold	4.0W/mK	0.18mm	1.82
5	Overmold	4.0W/mK	0.15mm	1.61

Table 1: Thermal simulation DOE for overmolded and exposed lidded package

III. Backside Metallization (BSM)

The package backside metallization process is similar to EMI (electromagnetic interference) shielding where a thin layer for metal shielding is applied at the last stage of package assembly process. Typically, SUS Cu layers are used in the shielding process with thickness around sub-micron to a few micron levels. It is an inline sputtering process integrated with the assembly line. It has capability of six side sputtering with a side to top thickness aspect ratio >40%. Automated visual inspection is conducted to make sure sputtering thickness comfortably meet requirements. The simplified process flow for sputtering or metallization is shown below (Figure 5).

a. Film lamination on the frame
b. Laser cut to form a cavity on the film to makes sure there is no sputtering on the bottom side of the package
c. Package loading on the film cavity
d. Metal deposition on the package top and sides
e. Package unloading to JEDEC tray

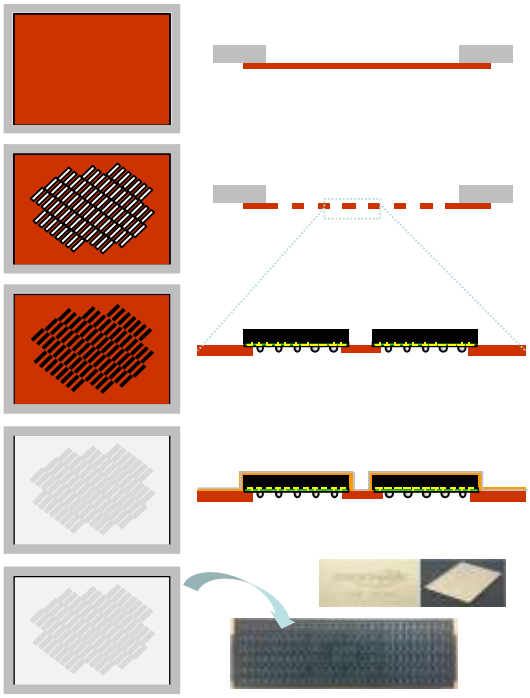

Figure 5: Typical metal sputtering process flow

This package backside metallization process has already been qualified for numerous programs with single die, multi die packages and different body sizes for many applications. Initial work was conducted on an 8X8mm fcCSP LGA (land grid array) package with 4X4mm die size. It was an exposed die molded package with Cu pillar bump using a 3L coreless trace substrate. Various literatures already have proved that Cu pillar bumps enhance both electrical and thermal performance of the package. Published literatures also proved that Cu pillar with bond on trace is superior for electrical and thermal and finally, it is a lower cost solution than the standard solder mask defined pad. Thermal study has been conducted on 8X8mm fcCSP with backside metallization followed by solder TIM and heatspreader as opposed to similar package with standard heatspreader package without metallization. Thermal measurement data found that as high as 30% thermal improvement was observed in the backside metallization package.

As the package size and die size increases, the effect of package backside metallization may not be as significant of a factor. Thermal analysis was performed on a larger body size (17X17mm with 10X10mm die size) fcCSP to understand the thermal performance of a backside metal package against standard a heatspreader package. An exposed molded backside metallization package with and without heatspreader conditions is shown in Figure 6 below. Thermal transient analysis was performed to understand the effect of backside metallization. In both the packages, solder TIM is used between die to heatspreader and heatspreader to heatsink. Theta ja (junction to ambient), and junction temperature are simulated and shown in Table 2 below. Almost no difference was found in theta ja between the two legs. It is proved that an expensive heatspreader is not needed to dissipate heat and that a thin layer of backside metal is good enough to comfortably mitigate thermal issues in the package.

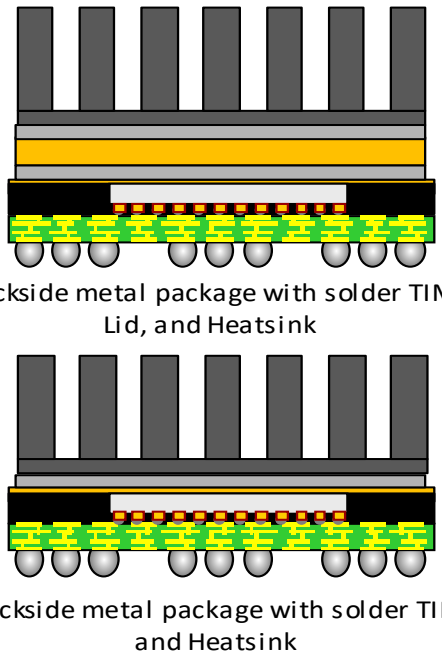

Figure 6: Exposed die molded fcCSP with solder TIMs, Heatsink, and with or without lid

Ambient Temperature (°C)			25 °C			
Power			1 W			
2m/s airflow			$T_{J\text{-}max}$	T_T	T_B	Q_{JA}
Package type	TIM1	TIM2	(°C)	(°C)	(°C)	(°C/W)
BSM with lid	Solder	Solder	27.93	27.91	27.26	2.93
BSM no lid	X	Solder	27.97	27.96	27.27	2.97

Table 2: Thermal simulation data for a fcCSP BSM package with and without lid condition

IV. Conclusion

With the phenomenal expansion of fcCSP demand in the industry due to superior performance in thin and small form factor package, assembly suppliers are positioning themselves to support the strategic need for very cost effective, high performance packages for various demanding applications. Thermal is one of the key challenges in these cost sensitive application areas. With the evolution of thin backside metallization, the package requirements can be comfortably achieved at a significantly lower packaging cost versus a heatspreader package. This solution is comprehensively qualified and running in high volume production for various application types in the industry.

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