The New Technology Solutions for Advanced SiP Devices

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For many years, System-in-Package (SiP) technology has been a focus for semiconductor packaging to address the ongoing market trend of system integration and size reduction. Today's increased complexity and higher package density for SiP devices has driven the development of new packaging technologies. In response, compartmental shield technology makes it possible to put several functions into a single SiP without interference among the chips and double-side assembly technology greatly increases the chip density. More challenging requirements from customers in high technology markets require even further research into SiP technology. This report will discuss technologies that are currently being applied to SiPs and forecast what to expect in the future.

Introduction

To better understanding System-in-Package (SiP) technology, it is necessary to review why SiP market share has dramatically increased, which areas require focus for future SiPs and what kinds of solutions are available for advanced SiPs. There are several advantages in SiPs, such as time to market, integrated function with good yield, miniaturization, cost saving and reliability.

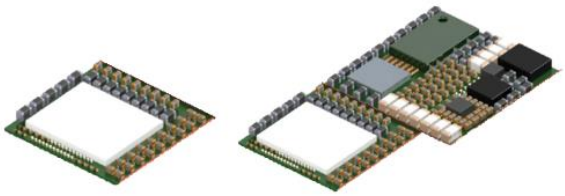

Fig 1. Function integration in SiP

Regarding time to market, customers required very short development time prior to production. To get better performance, passives around the die were changed to achieve the required functionality without revising the die which would require more time. That is specifically why SiP design was selected for RF devices which require fine tuning to meet the demanding specifications from customers.

To implement complex functions, the integration of technology for each function is required. With SiPs, this integration happens within the package. For complex products, SiPs provide good yield since faults in individual components are rejected at the die level prior to installation in expensive packages. For improving the yield during production and reducing these types of rejects, end customers prefer the SiP devices which place small components in the package and not on the main board.

SiP is physically larger than the equivalent system on chip (SoC) configuration. However, SiP offers substantial size reduction benefits as compared to the component integration occurring at the system board level. The placement of many components in SiPs occurs at high speeds – greater than 20 times faster than conventional chip attach machine for PNP transistors.

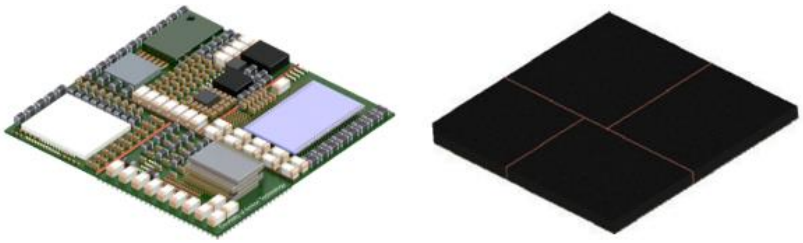

Figure 2. SiP with compartmental shield

Recently, drop testing has become very important due to the increased requirements of portable and wearable products. Small components on conventional boards have problems in drop tests. So, some customers have requested the application of an over mold on components with compartmental shield for preventing electrical interference.

Market Trend of 5G

Figure 3 shows the market outlook for smartphone SiPs in 5th generation (5G) wireless communication technology. Continued advances in wireless communication technology have required more SiPs in smartphones. With 1G wireless technology, voice communication was possible. With 2G, text with voice communication was possible. Advances to 3G allowed internet usage with very slow speed and the introduction of the smartphone. For 4G, the speed is almost same as wired technology. So, internet gaming and various applications including, video communication were possible and made the smartphone a must for everyday life. Companies such as Netflix, YouTube and Uber were launched and/or dramatically increased with 4G. With 5G technology, autonomous vehicles, augmented reality (AR), virtual reality (VR) and numerous Internet of Things (IoT) applications become possible.

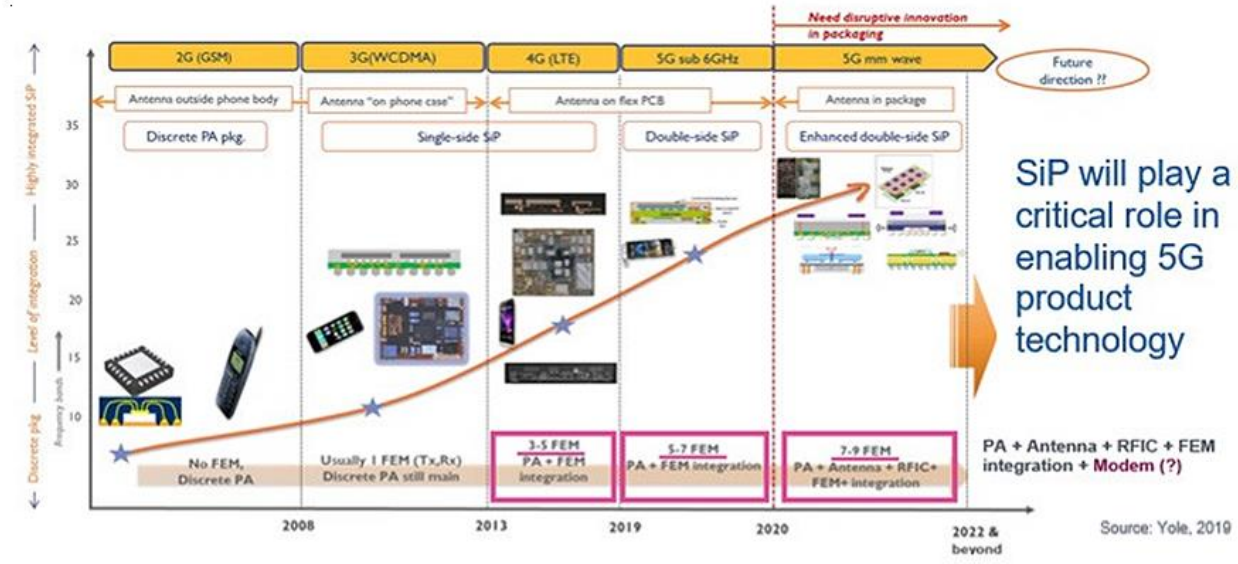

Figure 3. Market outlook for smartphone SiP Packages

What is different with 5G technology compared to 4G? Until 4G, wireless communication technology was mainly applied to smartphones. With 5G, it is not only used for smartphones but also for automotive, consumer and computing (network) market segments. This increased usage will require

improvement of real-time response with 20 times faster data transfer speed and low latency of ~ 0.001s. Low latency is one of the biggest features to enable autonomous vehicles. It also allows mass connection technology with things as well as people. However, with the transition from 4G to 5G, everything will not change at once. Like 4G implementation, incrementally improved platforms will be announced, which will require assembly packaging development time to accelerate.

Figure 4. System integration methods

With SoC technology, the integration of electronic circuits on chip is possible – the highest integration and better performance. However, it is not easy to implement SoCs due to high non-recurring engineering (NRE) cost, long development time, difficulty in fine tuning and a high technical threshold.

In contrast, System-on-Board (SoB) is the integration of packages on the printed circuit board (PCB). It was a very popular with 3G technology where the wireless communication speed is slower than wired communication technology. It has flexible integration and short development time. However, it also has disadvantages, such as requiring more area for system implementation and higher cost from yield loss, which, with more advanced technology applications, increases the cost of yield loss. With the application of 5G technology, the requirement for SoB goes away.

SiPs integrate active and passive components within the package. With heterogeneous integration, it is possible to miniaturize without high NRE and fine tune to avoid long development times. SiPs also have a disadvantage of assembly yield loss by increased integration of smaller areas.

Current SiP Solution

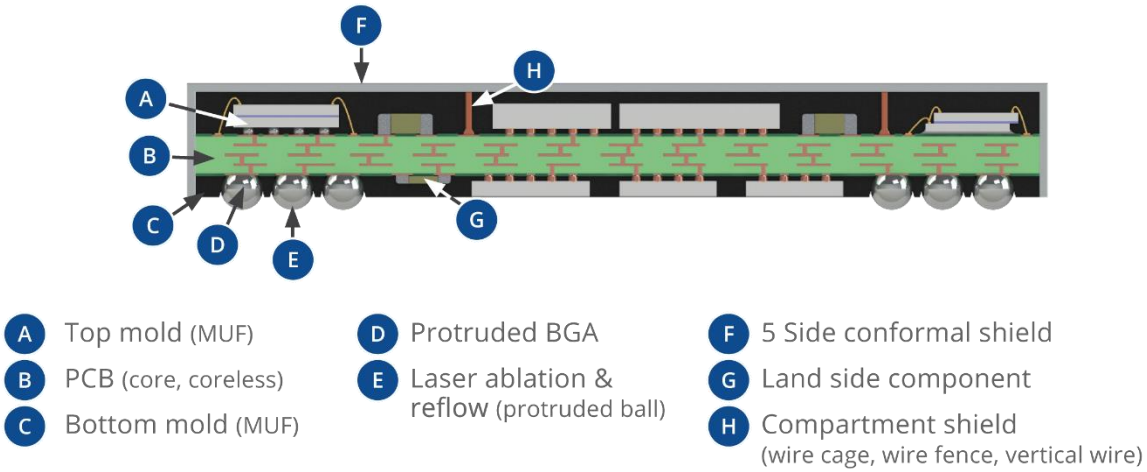

Figure 5. DSMBGA structure

Today, a Double-Sided Molded Ball Grid Array (DSMBGA) SiP is what customers want to use in their products (see Figure 5). Just one year ago, the double side assembly without mold on the bottom side was introduced to market. However, observed failures in drop testing for mobile devices required a "keep out zone" for capillary underfill on flip chip (FC) die. Other problems include cracks on thin FC die during the bottom side surface mount technology (SMT) and an unstable electromagnetic interference (EMI) shield on the bottom area. The DSMBGA solved those problems.

Advanced design rules to integrate as many functions as the current technology allowed was applied on the top side. Fine-pitch flip chip die with molded underfill, passives which have lower height than the thin FC die and compartmental shield to prevent the electric interference on top side were implemented. Among these items, compartmental shield technology made the SiP more attractive to customers since it could integrate various functions within the package. A ball protrusion structure on the mold surface reduces the stress during the drop test and strip grinding technology makes thin die without the risk of cracking possible. An EMI shield on the package protects the sensitive system from nearby packages and it has driven the miniaturization for mobility products.

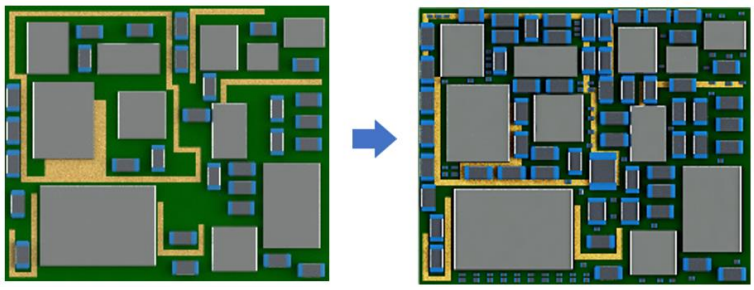

Figure 6. Advanced design rules

For higher integration through advanced design rules, advanced SMT module assembly is required to remove manual handling. Especially, after pick and place, the substrate should be fed to reflow without handling because even very minor misalignment can have a serious impact. Currently, laser assist bonding (LAB) technology was developed to prevent even minor handling during reflow. However, it needs further development for laser soldering through various materials which are not only Si but also ceramic, GaAs, epoxy molding compound (EMC), etc.

No matter how tight the design rules are, issues can occur beyond normal or abnormal control during mass production. For example, high-speed operations including the pick and place are difficult for quality control without manual handling inspection. With today's current advanced technology, real-time inspection tools such as a Solder Paste Inspection Machine and an Auto Optical Inspection machine were configurated into a SMT module to prevent massive defects during the SMT even if screening is not performed for defects after soldering.

For package-level integration, traceability of not only each part, but also each assembly condition, is required to define the root cause of a defect determined by a test site screen or reported by the end customer. As a customer requirement for traceability, a 2D barcode marking on the package was applied several years ago. However, it is still in development for detailed item traceability such as parts applied during assembly and die coordinates on a wafer.

The main reason it is difficult to apply tight and advanced design rules are solder bridge defect occurrences for each part during SMT assembly. To optimize the solder printing quality, it is not only important to have screen printer and stencil quality but also to have accurate stencil and footprint pad designs on the substrate and to implement a significant effort to reduce the mismatch between the substrate and the stencil.

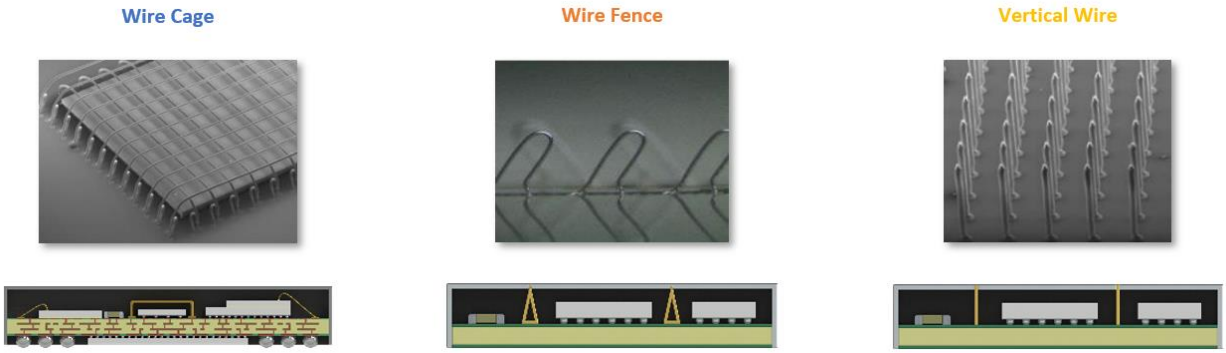

Figure 7. Compartmental shield method

With compartmental shield technology, it is possible to integrate various function in SiPs even though some parts are sensitive to electrical interference. Interference can be prevented by proper shield performance and geometry design.

For example, trench and fill technology was developed several years ago. It required a relatively large area to implement without voids occurring during filling and to achieve a stable trench shape. The filled material was connected to EMI shielding on the mold surface.

With wire cage technology, shielding is possible without an EMI shield on mold surface. The required area for shielding using this technology is smaller than a metal cover attachment. Wire fence technology is mainly applied with laser grooves on the mold surface. The wires exposed by laser grooving are connected to EMI shielding on the mold surface.

Finally, there is customer interest in vertical wire technology because required space is smaller than other technologies and it can implement fine pitch on a narrow trace.

To reduce the space for exposing wire, strip grinding technology is used instead of laser grooving which affects the clearance between the component and laser-grooved surface.

Discussion

Embedded components into substrate technology was applied to some devices even though it required development for yield improvement. Also, conformal and compartmental shield technology have been used for SiP integration. Double-side assembly technology made high integration possible by populating components on both planes. The 5G antenna, which is very important for 5G technology, was initially developed for a SiP structure.

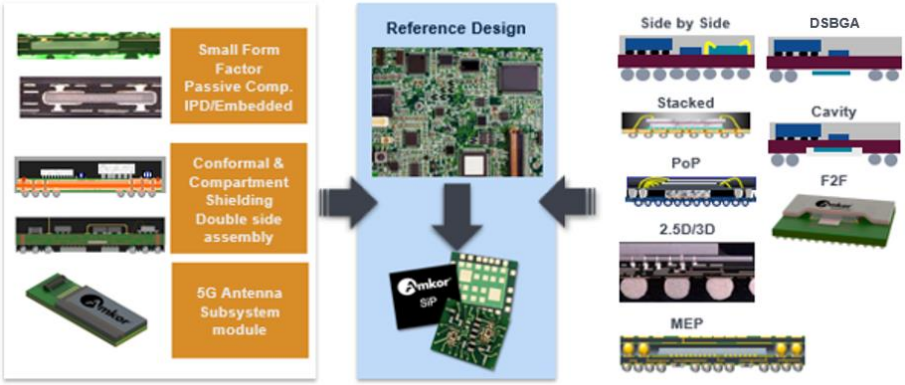

Figure 8. Next applicable structure for SiP

The developed compartmental shield technology allows increasing integration of various functions in SiPs.

Reducing the X /Y and Z package size is possible to achieve with existing assembly package technologies, which are Package-on-Package (PoP), cavity structures, 2.5D /3D, package thinning by grinding and a molded embedded package (MEP). It can be assumed that populating components on multi-planes, such as MEP technology, will be applied to future SiP devices. Fine pitch I/O technology, even if components are placed on the same side, requires further development.

For further miniaturizing through high integration, thermal releasing and reliability issues must also be considered and addressed.

Conclusion

SiP technology integrates active and passive components within the package. With this heterogeneous integration, it is possible to miniaturization without incurring high NRE and reduce time to development by finetuning. However, it also has the disadvantage of assembly yield loss by higher integration of small area components.

For higher integration without yield loss, an advanced SMT module configuration is required for higher accuracy and stable quality control. However, no matter how tight the design rules are, issues can occur beyond normal or abnormal control during mass production. High-speed operations, including the pick and place, are difficult for quality control without manual handling inspection. With today's current advanced technology, real-time inspection tools such as a Solder Paste Inspection Machine and an Auto Optical Inspection machine were configurated into a SMT module to prevent massive defects during the SMT even if screening is not performed for defects after soldering.

With compartmental shield technology, it is possible to integrate various function in SiPs even though some parts are sensitive to electrical interference. Interference can be prevented by proper shield performance and geometry design.

Among the several shielding technologies, vertical wire technology requires less space than other technologies and it can implement fine pitch on a narrow trace.

To reduce the space for exposing wire, strip grinding technology is used instead of laser grooving which affects the clearance between the component and laser-grooved surface.

Reducing the X/Y and Z package size is possible to achieve with existing assembly package technologies. However, for further miniaturizing through high integration, thermal releasing and reliability issues must also be considered and addressed.

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Reference

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