S-SWIFT® Packaging with Fine Pitch Embedded Trace RDL

WonChul Do, VP, Fellow & Product Development Group Manager l Amkor Technology, Inc.

The needs of high-performance devices for artificial intelligence (AI), high performance computing (HPC) and data center applications have drastically accelerated during the Covid-19 pandemic period. At the same time, the integrated circuit (IC) industry struggles to minimize the silicon technology node to satisfy the endless requirements of computing performance within tight cost constraints. Currently, 2-nm node technology was introduced using the nanosheet technology. This design provides 45% increased speed with the same power usage of the 7-nm node. However, the design cost and development time to market (TMT) astronomically increase as the node size decreases and wafer yield is significantly lower because a tiny little defect can break the total function of single chip. Chiplet technology is one of most effective solutions to overcome these limitations and provide state-of-the-art product to the consumers with reasonable and affordable prices.

Chiplets separate the core blocks with advanced node size to small dies for improving the wafer yield and reusing the intellectual property (IP) of prior node blocks to reduce the design cost. To interconnect these heterogeneous block dies with different node size and different materials, advanced IC packaging technologies are required. Previously, the Multi-chip Module (MCM) Flip Chip Ball Grid Array (FCBGA) has been conventionally adopted as a heterogeneous interface of multi-chips on the laminate substrate. However, it was not suitable for advanced node ICs due to the significantly long electrical path of the substrate. A module interface with 2.5D Through Silicon Via (TSV) technology was introduced as the new candidate for high performance packages with an extremely short electrical path but its use was restricted by limited performance in high frequency (4-6 GHz) applications due to the limitations of silicon interposer [1]. Therefore, a High-Density Fan-Out (HDFO) interface, which excluded the silicon (Si) and inorganic dielectric and adopted an organic dielectric, has recently emerged. Specifically, Amkor Technology's HDFO is known as the substrate Silicon Wafer Integrated Fan-out Technology (S-SWIFT®) package providing higher bandwidth die-to-die interconnects for heterogeneous integration with a high-density interposer.

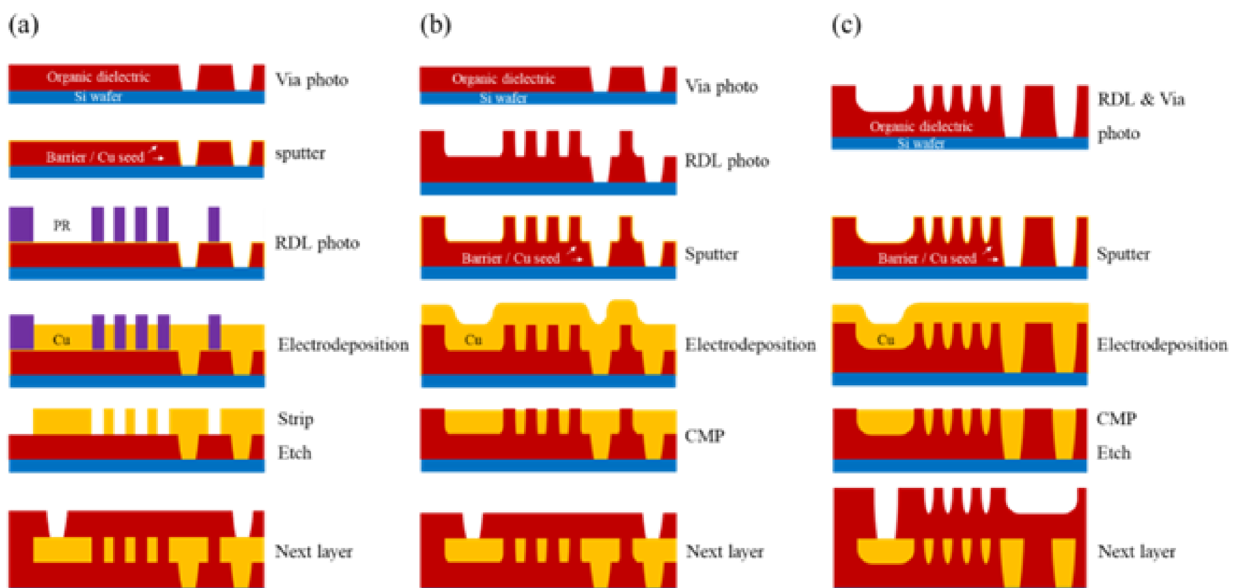

Figure 1. Schematic diagrams of RDL process flow by (a) semi-additive process (SAP), (b) dual damascene process and (c) new embedded trace RDL process.

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Its excellent performance already has been proven in previous research [1, 2]. Many critical design aspects needed to be addressed to demonstrate the S-SWIFT methodology, including: the fine pitch µ-bump interface, accurate warpage control of components during the thermal assembly process, capillary under-fill, over-molding technique, through mold interface (such as Cu tall pillar), mid-end of line (MEOL) process and the mold-side bumping process. A high-density redistribution layer (RDL) technique is one of core technologies necessary to demonstrate the viability of the HDFO interposer module. The RDL in HDFO provides the chip-to-chip interface and higher density RDL is required to interconnect the chips with smaller node size blocks. The semi-additive process (SAP) is used for manufacturing the RDL of the HDFO module.

However, SAP has a few challenges in defining the fine pitch features. Fine trace lines may collapse with a high aspect trace ratio, delamination can occur due to a small contact area to the substrate and the photoresist used as the template may remain in vias [3]. To overcome these issues, a dual damascene process with an organic dielectric has been proposed. The seed layer undercut issue could be prevented with the RDL embedded in the organic dielectric during the process. RDL with a dual damascene process by photolithography on the Ajinomoto build-up film (ABF) type polymer layer has been introduced [4]. The advantage of dual damascene RDL in high frequency applications was evaluated. Subsequently, a special patterning method for achieving the small via in dual damascene RDL was introduced [5]. Significantly high resolution RDL (500 nm) was achieved with the high numerical aperture (NA) (0.48) lithography tool. Polybenzoxazole (PBO) patterning using a combination of photolithography and dry etch for dual damascene RDL has also been researched [6]. Struggles to solve the cracking after the dry etch and high overburden after the Cu electrodeposition were discussed.

To overcome the challenges described above, an embedded trace RDL (ETR) process was developed and its patterning performance and verified reliability of ETR were demonstrated. To achieve the ETR, key process optimizations and material modifications were carried out. The S-SWIFT package, where an ASIC, high bandwidth memory (HBM) and the substrate were interconnected by ETR also has been demonstrated. The design elements have successfully passed JEDEC standard reliability tests.

The Capability of Embedded Trace RDL

SAP was conventionally used to fabricate the RDL of universal packages and its standard process flow is shown in Figure 1 (a). Firstly, liquid type photo-imageable organic dielectric was spin coated on the carrier wafer and the via patterns were aligned by photolithography. To enable the electrodeposition of the Cu RDL, a barrier and the Cu seed layer were deposited on the post-cured dielectric film by a sputter process. The RDL patterns were aligned on the seed layer following the photoresist (PR) process and Cu RDL was electrodeposited. Finally, the PR template and Cu / barrier layer was striped and etched sequentially. As noted previously, SAP is mainstream technology as an RDL solution for universal IC packages due to its convenient and reliable process performance. However, downscaling of RDL with SAP has challenges such as seed layer under cut or side wall etch issues [7].

These challenges could be addressed by embedding the trace in the dielectric layer without an etch process. As presented in the Figure 1. (b) and (c), the dual damascene Cu is embedded in the organic dielectric pattern by electrodepositing the Cu on the preformed passivation layer and removing the Cu overburden. This structure has no Cu collapse risk, no sidewall etch issue and the three-side faced barrier metal has enhanced reliability. Moreover, the dual damascene Cu structure has advantages in terms of high frequency signal pass characteristics, because the three-side faced smooth Cu surface is less affected by electron scattering even if current is concentrated at the shallow RDL surface by the skin effect in high frequency signals. [4] Process flow to form the dual damascene structure with RDL and via on the organic dielectric film is indicated in the top side of Figure 1 (b). The via and RDL structures were separately formed by a two-pass photolithography process which includes the spin coating of organic dielectric material, soft-bake, ultraviolet (UV)-exposure, develop and thermal cure process.

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The previous process was simplified by adopting the novel photolithography technique. As indicated in the top side of Figure 1 (c), the via and RDL patterns could be formed by a single-shot of UV-exposure on the thickly coated organic dielectric film. This method reduces the number of RDL process steps by 40% compared to the current dual damascene method and even reduces 33% compared to the SAP. Accordingly, the process cost also could be reduced. In addition, since the via and RDL could be formed by a single-shot of UV exposure with a specially designed mask, misalignment between the via and capture-pad could be avoided.

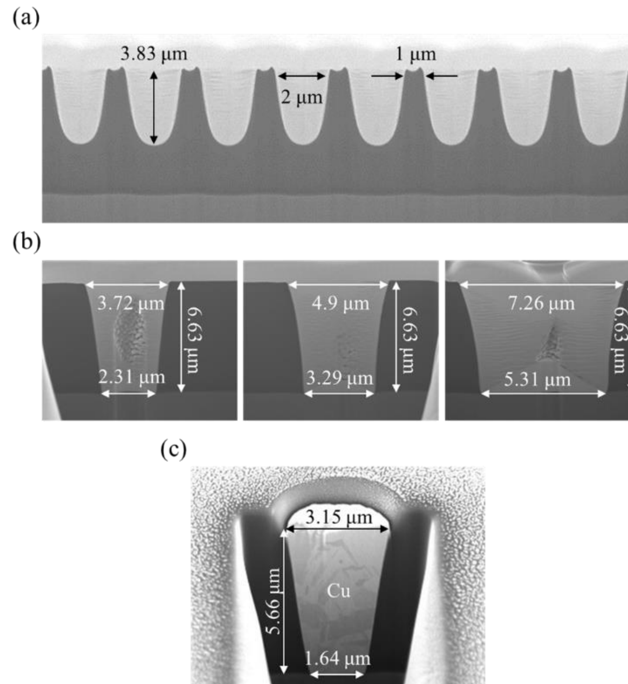

Figure 2. (a) RDL patterns with 2-µm line width and 1-µm space, (b) via patterns with various radiuses which were formed by embedded trace RDL patterning and (c) the smallest size via with the embedded trace RDL process.

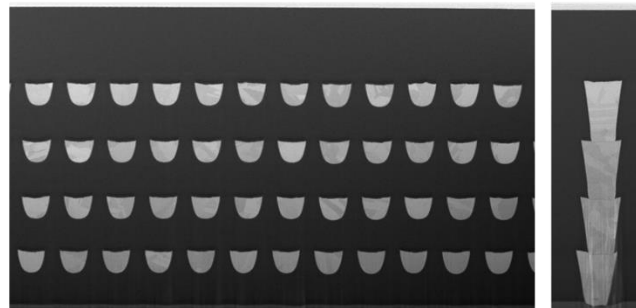

Figure 3. ***Cross-sectional images of a 4-layer RDL with 2/1 µm of line width/space and a 2-µm stack via formed by the ETR process.***

The patterning capability of new ETR process is indicated in Figure 2. Trench patterns for RDL with 2/1 µm line/space (Figure 2 (a)) and various size via patterns (Figure 2 (b)) could be formed. Minimum resolution of via with ETR is 3.15 µm at the top and 1.64 µm at the bottom as shown in Figure 2 (c). This method is advantageous in terms of advanced circuit design as well. A capture-pad for the via is required at the RDL layer to supplement the lay-out accuracy of the align tool during the stacking

of the via and RDL layer, while it was not required for the ETR process. Therefore, additional area could be used for the RDL and RDL density could be increased.

Figure 3 shows the RDL layer stacking capability of the ETR process. Since the fine RDL pattern was formed on the top of dielectric film and each layer surface is flat, significantly stable layer stacking is possible with the ETR process. Four layers of RDL with 2/1-µm line/space and stacked pad-less via with 2-µm critical dimension could be obtained with the ETR process.

Key Process Development

To achieve the ETR process, delicate control of process parameter is required from the start with the spin coating of organic dielectric film. The extreme uniform coating technique was developed to prevent the metal residue that occurred at chemical-mechanical polishing (CMP) shadow formed in ununiform coating region of organic dielectric film. Figure 4 shows the change of cross-sectional thickness profile of organic dielectric film as the level of extreme uniform coating factor changed. In the case of uniformity level 0, the extreme uniform coating is not applied. A coating height difference of 0.26 µm occurred from the wafer edge to the 180-mm portion resulting in CMP shadowing. Consequently, thick Cu residue remained at the wafer edge after the Cu dual damascene process, although the center region is clear. As can be seen from the whole wafer and magnified image in the Figure 5 (a) and (b), RDL circuits at the wafer edge were shorted.

The CMP shadow at the wafer edge was diminished as the extreme uniform coating level increased. The concave type curvature coating profile with extreme uniform coating level 1 was decreased as the extreme uniform coating level increased to level 3, and it changed to the convex type coating profile with no CMP shadow by adopting the extreme uniform coating level 4. Moreover, the total difference of film thickness was reduced from 0.47 µm with no extreme uniform coating to 0.12 µm with extreme uniform coating level 4. Since the CMP shadow was diminished by the extreme uniform coating, the Cu residue did not remain at the wafer edge after the dual damascene process. This is shown in Figure 5 (c) and magnified image at the wafer edge is in Figure 5 (d). Consequently, very high yield was achieved by applying the level 4 coating recipe that significantly improved the coating uniformity.

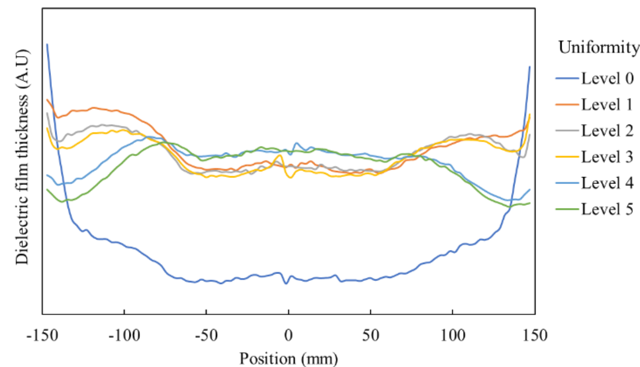

Figure 4. Cross-sectional profile of dielectric film with extreme uniform coating level

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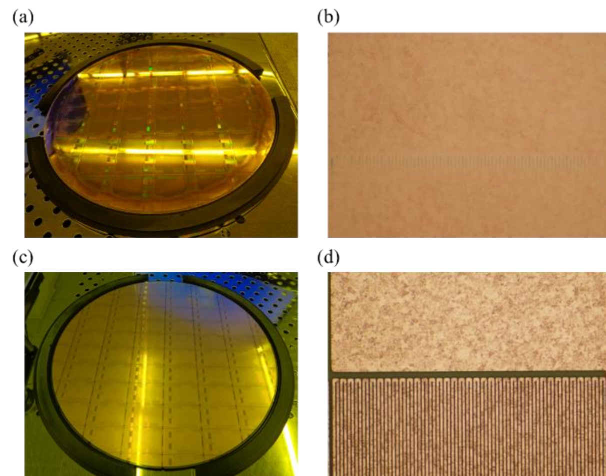

Figure 5. Optic images of a wafer after the ETR process: (a) without extreme uniform coating, (b) Cu residue at the wafer edge, (c) with extreme uniform coating and (d) clean RDL pattern at the wafer edge.

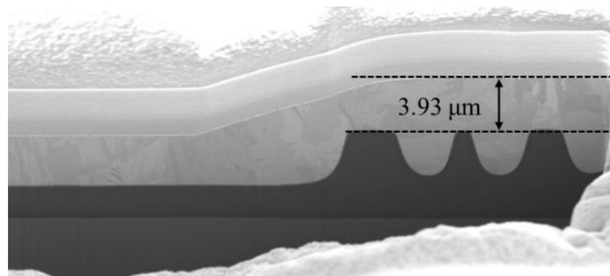

Figure 6. Cress-sectional image of Cu electrodeposited structure on the ETR pattern.

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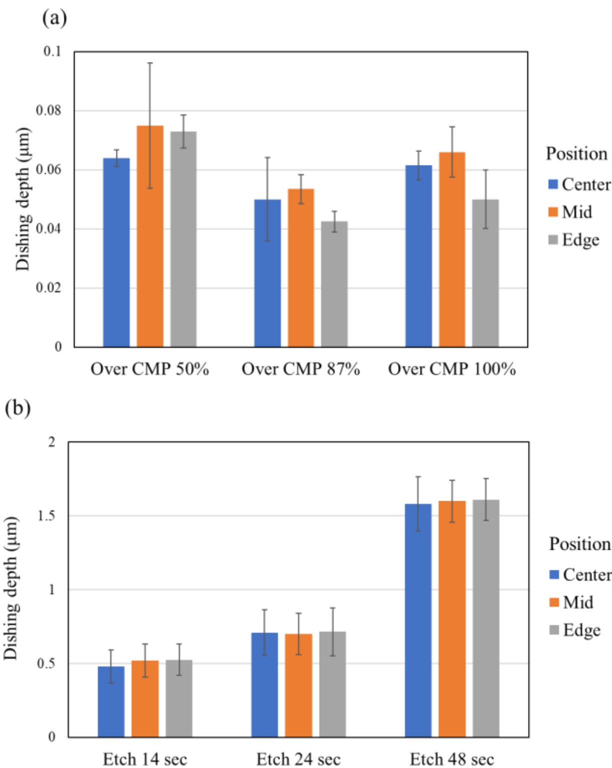

Figure 7. Dishing depth of Cu in the ETR pattern after the (a) CMP with over-CMP ratio and (b) following Cu wet-etch process with etch time.

Figure 6. shows the cross-sectional image of the Cu electrodeposited ETR structure which had wide and fine RDL mixed pattern. Fast Cu filling is possible in the narrow trench structure for fine RDL and small via pattern because the accelerator in the plating bath is concentrating on the large curvature region of Cu growing surface and it decreases the curvature [8]. Originally, this via filling principle was applied only to small via in the SAP method but in the dual damascene process, it is also applied in the narrow trench structure. However, via filling does not work for the large trench in the wide RDL because there is no region with large curvature for concentrating the accelerator species excluding the trench corner part. Therefore, the plating rate at the trench bottom is almost parallel with the top surface and a thick overburden layer at the top surface is inevitable to fill the wide RDL. Accordingly, a large amount of Cu CMP is required.

The Cu CMP process for dual damascene process is typically performed by 3 steps with 3 CMP platens: (1) bulk Cu removal, (2) Cu polishing and (3) barrier and oxide layer removal. In the ETR process, the Cu removal process was simplified by combining the Cu CMP with single CMP platen and wet-etch process. This method is advantageous in reducing process cost and increasing the process speed. Firstly, bulk Cu removal was performed with a high-speed Cu CMP process using a single CMP platen. Almost 4 µm of Cu overburden layer was rapidly removed with a 900 nm/min removal rate. In this situation, delicate control of CMP uniformity is difficult over the whole wafer region. Thus, over-CMP to finish the bulk Cu removal of the whole wafer surface is inevitable and role of the stop layer is important to prevent over-CMP related issues such as over-dishing or vanishing of metal or dielectric layer. Figure 7 (a) shows the wafer regional dishing depth is uniformly controlled and not over 90 nm regardless of the over-CMP ratio because the CMP-stop layer limits the over-CMP.

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Cu residue which remained after the CMP and barrier layer was removed by a cost effective wet-etch process, instead of step CMPs. Cu residue was clearly removed by Cu wet-etch process. Moreover, additional Cu RDL height control is possible because Cu dishing could be uniformly controlled by etch-time, as shown in the Figure 7 (b). Finally, the barrier layer is also clearly removed by a standard wet-etch process.

S-SWIFT Demonstration

The S-SWIFT demonstration with ETR was performed with a standard S-SWIFT assembly flow as shown in Figure 8 [1]. Four layers of ETR were stacked on the silicon wafer and the lead-free solder μ-bumps were electrodeposited on top of the ETR. Multi-chips with ASIC and HBMs were aligned on the μ-bumps and attached by a mass reflow process. Next, capillary under-fill was carried out between the ETR and multi-chips. Following this, the mold process was carried out with an epoxy mold compound (EMC) on the attached chips and mold-grinding was then performed for exposing the multiple chips to contact the thermal interface material (TIM). A 2nd carrier wafer was attached on the front-side of the HDFO with an UV-detachable adhesive and the backside wafer was removed by a combination of wafer-grinding and a dry-etch process to form the Cu pillar on the backside. After the Cu pillar and lead-free solder electrodeposition, the carrier wafer was removed by an UV laser and the wafer saw process was carried out. Individual modules were attached on the laminate substrates and an under-fill material was applied between the module and substrate. Then, the lid was attached on the front side of the S-SWIFT module with TIM material and the solder balls were attached at the backside.

Figure 9 shows the sequential images of the S-SWIFT assembly process. Even though the standard assembly parameters for SAP were used without any modification, S-SWIFT assembly was successfully demonstrated without any issues. If a different RDL fabrication method and different organic dielectric material were used for the HDFO module, they may not significantly affect the assembly process due to the small difference of mechanical characteristics and the available structural area in the package. It was identified that all bumps in chips and substrate were well attached on the HDFO module through the cross-sectional images in Figure 10. Although not presented in this paper, it also has been confirmed by X-ray analysis and scanning acoustic tomography (SAT) as well. Therefore, it could be concluded that the heterogeneous interconnection of multi-chips and substrate was achieved by S-SWIFT packaging with ETR.

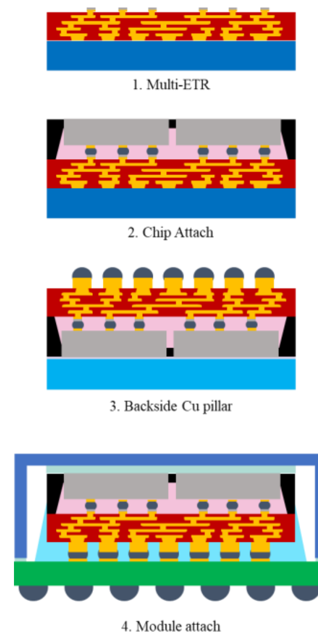

Figure 3. Process flow of S-SWIFT.

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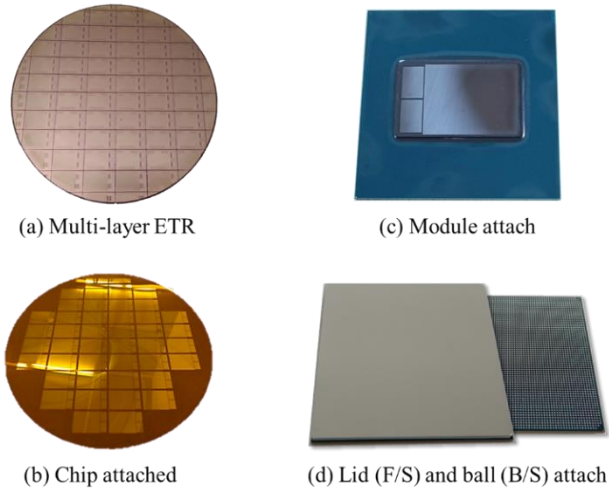

Figure 3. Optic images of the S-SWIFT demonstration: (a) after the 4-layer ETR formation, (b) after the mold grinding with attached chips, (c) after the HDFO module attached on the substrate and (d) after the lid attach at front-side and ball attachment at the back side of the S-SWIFT package.

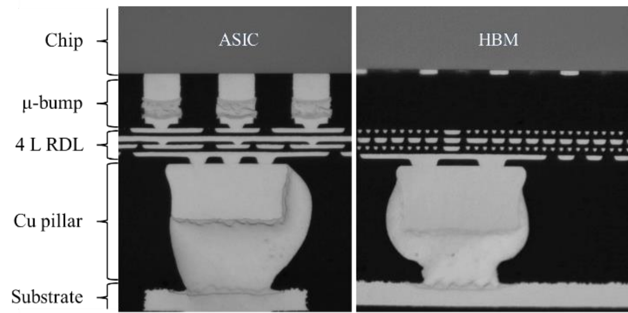

Figure 3. Cross-sectional images of the S-SWIFT module with 4-layer ETR..

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Reliability Performance

Since the seed layer surrounding the three faces of the ETR acts as a barrier, the structure of the ETR has advantages in terms of reliability affected by current, heat and humidity. Especially, the layer prevents Cu ions from migrating into the passivation layer from current flowing during the Biased Highly Accelerated Stress Test (BHAST).

Two layers of ETR with a comb structure circuit were fabricated to verify the Cu ion migration characteristic. BHAST was performed for 96 hours with 3.3 V applied between the comb circuit with 85% humidity and 130°C conditions. A prototype organic dielectric material was used in this test. After BHAST, most of comb circuits were shorted by Cu ion migration from the top of ETR without barrier layer. (Table 1)

Dielectric Material	Process conditions	b-HAST Conditions	Read point	Sample size	Result
Prototype	Before optimization	3.3V/130°C/85% RH	96 hours	22	Fail
Modified	After optimization	3.3V/130°C/85% RH	96 hours	22	Pass

Table 1. B-HAST Test Results with Organic Dielectric Film Process Conditions.

The Cu ion migration phenomenon inside the organic dielectric material during BHAST is similar to the electrodeposition of metal [9]. Cu at the anode of comb circuit was ionized by 3.3 V of anodic potential and migrated to the cathode of comb circuit through the water inside the organic dielectric material with temperature supporting the process. The Cu ions were reduced to Cu by cathodic potential at the cathode of comb circuit. This chain reaction made the dendritic Cu electrode between the comb circuit, and it caused the short failures. Originally, the reaction could be controlled by controlling the diffusion of the reactant. First, process conditions were controlled to prevent the water adsorption inside the polymer. As a result, water absorption decreased with optimum process conditions. Next, dielectric material improvement was carried out to prevent the ionization of Cu by anodic potential. Therefore, anodic reaction of Cu and diffusion of reactant by water was suppressed. As a result, as shown in Table I, BHAST passed with samples fabricated with modified organic dielectric material and the use of improved RDL process conditions. These modified dielectric material and optimized process conditions were used to successfully demonstrate the viability of an S-SWIFT package with 4- layer RDL.

Test Item	Conditions	Read Point	Sample Size	Result
MSL4	30°C/60%RH, 245°C x3	Precon	22	Pass
T/C G	-40°C ~ 125°C	1500 cycles	22	Pass
u-HAST	110°C /85%RH	360 hours	22	Pass
HTS	150°C	1000 hours	22	Pass

Table 2. B-HAST Test Results with Organic Dielectric Film Process Conditions.

Reliability tests were performed to evaluate the ETR structure in the S-SWIFT package. All conditions in the reliability tests including the moisture soaking level 4 (MSL4), temperature cycling test condition G (T/C G), Unbiased Highly Accelerated Stress Test (UHAST) and the high temperature storage (HTS) test complied the JEDEC standard. As shown in the table II, all samples passed T/C G 1500 cycles, UHAST 360 hours and HTS 1000 hours.

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Conclusion

The embedded trace RDL has been developed as an RDL fabrication process for advanced High-Density Fan-out packaging that utilizes a novel photolithography technique with reduced cycle time and structural advantages. It provides an effective way to implement multilayer RDLs with less than 2/1 µm of line/space and vias without capture pads. The ETR's stacking capability has been confirmed up to 6 layers thanks to the flatness of the RDL layer. Innovative in unit process technique such as uniform coating, CMP and wet-etch were performed to fabricate the ETR. Through efforts to modify dielectric material and optimize process conditions, reliability in HAST could be improved.

Finally, S-SWIFT packaging was successfully demonstrated by heterogeneous integration of the ASIC and HBMs with ETR technology and Flip Chip assembly. The assembled units passed industry-standard component level reliability requirements.

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Additional Authors:

SangHyun Jin, R&D; JinSuk Jeong, R&D; YunKyung Jeong, R&D; YunKyung Jeong, R&D; JinYoung Khim, R&D l Amkor Technology Korea