Next Gen Laser Assisted Bonding (LAB) Technology

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In the semiconductor market, there are many applications including smartphone, tablets, central processing units (CPUs), artificial intelligence (AI), data cloud and more that are expecting rapid growth. Among them, CPU data processing, AI and data cloud require much higher power consumption than smart phone or tablets. For the higher power applications, Flip Chip ball grid array (FCBGA) or 2.5D packages with high thermal performance are expected to be the appropriate packages. For the FCBGA package, a heat spreader and thermal interface material (TIM) are used for thermal performance enhancement. Currently, polymer-based materials are commonly used as TIM1 (between die and the heat spreader) for heat conduction [1]. Even though a polymer-based TIM is widely used for FCBGAs, this material is not enough to cover high thermal applications.

For better TIM performance, a metal TIM is considered as a significant improvement. Among the various metals, indium or an indium alloy were recommended with their low melting point in a previous study [2]. To use a metal TIM, backside metallization (BSM) must be performed on both the silicon (Si) die and the lid surface because the metal TIM bonds with Si die and metal Lid by intermetallic bonding as shown in Fig. 1.

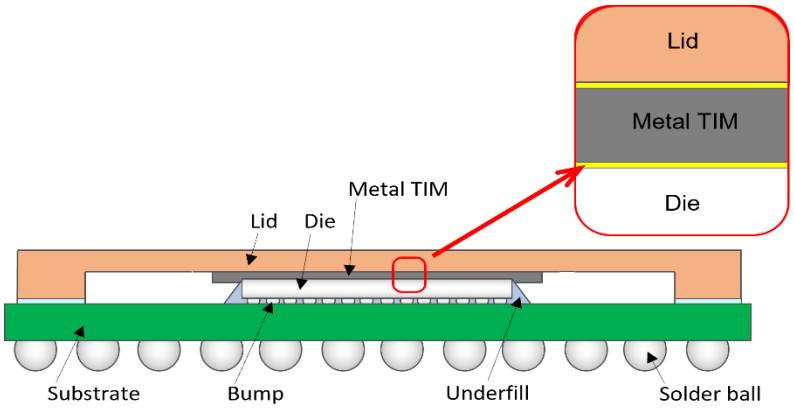


Figure 1. Schematic image of metal TIM on FCBGA.

From the viewpoint of the bump interconnection methodology, mass reflow (MR), thermocompression bond (TCB) and laser assisted bonding (LAB) are used in industry. For LAB, the technology and bonding mechanism have been reported and a general comparison of bonding methods is shown in Table 1 [3]. The focus of this new study is on LAB technology for the BSM die bump interconnection. Next Gen LAB technology is introduced to overcome the limitations of the existing LAB technology. Additionally, LAB process margin was checked based on optimized key LAB parameters. Furthermore, parts were built with LAB Process of Record (POR) conditions and submitted to reliability testing with bump joint cross-sectional analysis performed for any thermal degradation post reliability.

Process	Mass Reflow	TCB	LAB
Productivity	Highest productivity	Lowest productivity	High productivity
Bonding time	Longest bonding time (5~10min)	Short bonding time (a few sec)	Shortest bonding time (less than 1 sec)
Thermal stress	Highest thermal stress	Lowest thermal stress	Lower thermal stress
Warpage control	High warpage risk	Lowest warpage risk	Lower warpage risk

Table 1. Comparison table of Flip Chip bonding methods.

Test Vehicles

The test vehicle is an FCBGA package. The package body size is 45 mm x 4 5 mm and the silicon die size is 19.2 mm x 19.2 mm. Bump pitch is 165 µm with an 85 µm circular bump diameter. The total bump height is 60 µm by 40 µm for the copper (Cu) pillar bump with a 20-µm tin-silver (Sn-Ag) solder cap. The die backside metallization is finished with gold (Au). The organic substrate has six Cu layers, a Solder on Pad (SoP) finish and the total thickness is 1.07 mm. Additional information for the test vehicle is summarized in the Table 2.

	Items	Information
Package	Package type	FCBGA
	Package body size	45 x 45 mm^2
	Total height	3.48 mm
Die	Die size	19.2 x 19.2 mm^2
	Die thickness	550 µm
	Bump pitch / Count	165µm / 12312
	BSM (Back Side Metal)	Au finish
	Bump diameter	85 µm (Circular)
	Bump height	40 µm Cu/20 µm SnAg CAP (Total 60µm)
Substrate	Layer count	6 layer
	Total thickness	1.07 mm
	FC Pad finish	SOP

Table 1. Comparison table of Flip Chip bonding methods.

Experimental Details

Result with existing Top LAB for non-BSM die

Prior to the evaluation for the BSM die, the existing top LAB condition with non-BSM die, which is normal silicon die, was evaluated. POR conditions showed no abnormality at bump interconnection. Both X-ray inspection and bump cross section show no non-wet or bump short conditions as shown in Fig 2.

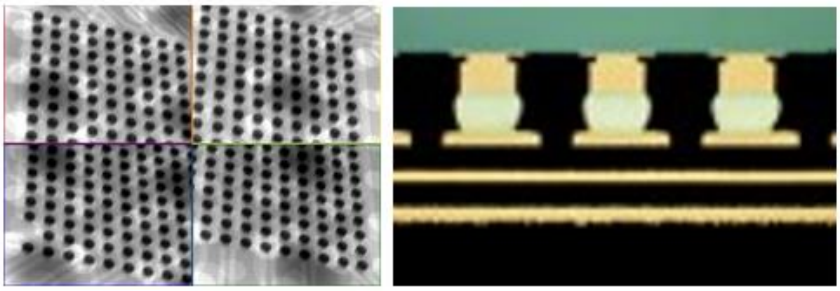


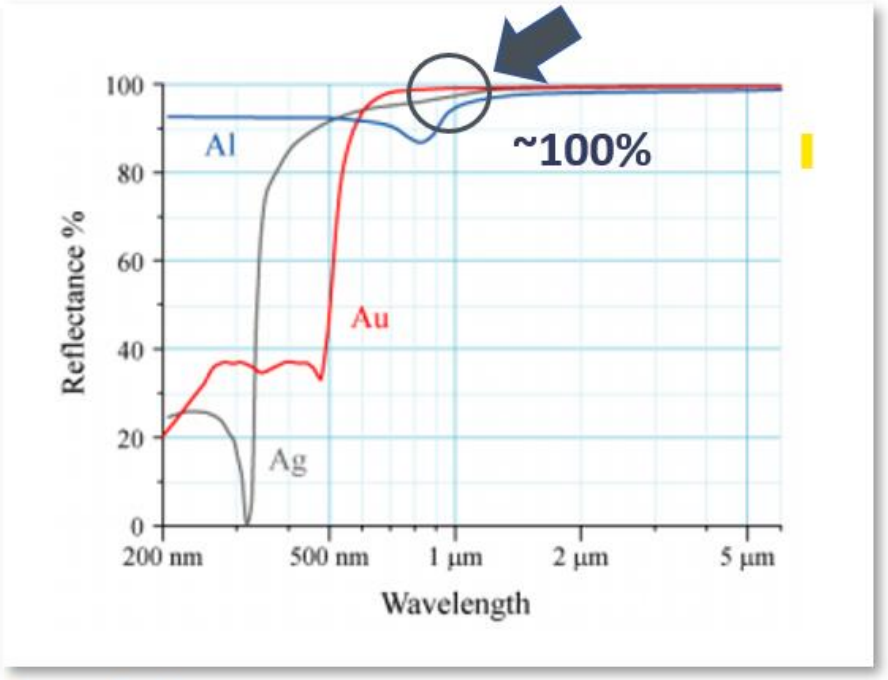
Figure 2. X-ray & bump X-section of non-BSM die.

Result with existing Top LAB for non-BSM die

Initially, the non-BSM die's POR LAB conditions were applied to the BSM die. However, the bump interconnect did not fully form, and die separated from the substrate. The reason is due to a high ratio of laser reflectance of the Au metallized surface of the silicon die. As shown in Fig. 3., Au's reflectance is almost 100% at the infrared (IR) wavelength. Next, 3X to 4X higher power was applied with same bonding time in Leg 1 to Leg 3. The 4X high power (Leg 3) shows no non-wet but the substrate surface is burned due to abnormally high power. The 3X power (Leg 1) shows no substrate surface damage but bump non-wet was observed by cross-sectional analysis. An intermediate point, the 3.5X (Leg 2) shows both bump non-wet and substrate surface damage.

As a next step, longer LAB time was applied with the same power. Leg 4 to Leg 6 used 12X to 16X longer time. All 3 legs show no substrate burn out but detected a bump non-wet cross section even at the longest bonding time. Summarized results are described in Table 3. The X-ray image and bump cross-section images are shown in Fig. 4.

Based on the results, it is very difficult to find optimum LAB conditions and acceptable process margin for mass production. The existing LAB technique cannot be recommended for BSM die bump interconnection due to the non-wet risk. This motivated the search for a new bonding method.

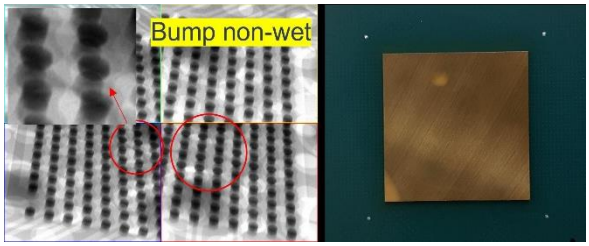


Source: optocity.com

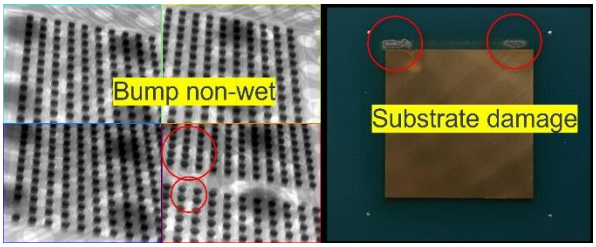
Figure 3. Reflectance (%) of metals vs. wavelength.

	LAB condition	Bump non-wet	Substrate damage	Remark
Leg 1	3X power	Yes	No	Higher power than POR Time fixed as POR
Leg 2	3.5X power	Yes	Yes	
Leg 3	4X power	No	Yes	
Leg 4	12X time	Yes	No	Longer time than POR Power fixed as POR
Leg 5	14X time	Yes	No	
Leg 6	16X time	Yes	No	

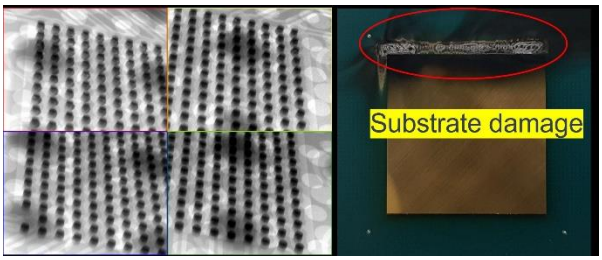
Table 3. Result of each leg with existing LAB.



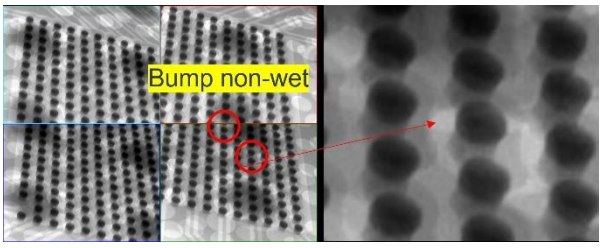
Leg1 : 3X power.



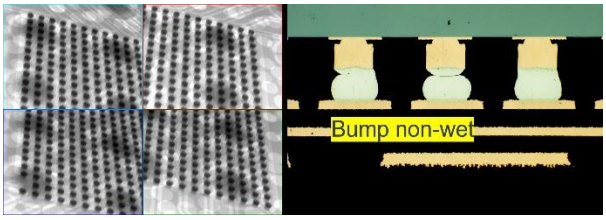
Leg 2 : 3.5X power.



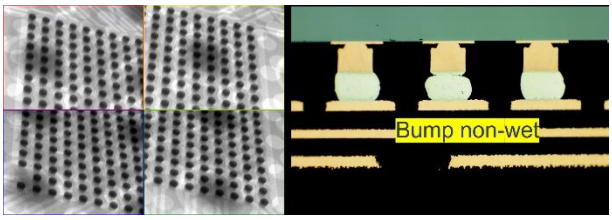
Leg 3 : 4X power.



Leg 4 : 12X time.



Leg 5 : 14X time.



Leg 6 : 16X time.

Figure 4. X-ray, cross section and substrate visual inspection image of each leg with existing LAB

Introduction of Next Gen LAB

To avoid the high reflectance of the metallized surface for BSM, a reverse type LAB, laser emission from bottom BGA side to bump by transmission through stage block, was proposed. This Next Gen LAB should overcome the limitations of existing LAB. Target applications would be BSM die, high bandwidth memory (in an epoxy molding compound (EMC) package) and 2.5D module interconnections. Fig 5 shows schematic images of the existing Top LAB and the Next Gen LAB (Reverse LAB) in detail.

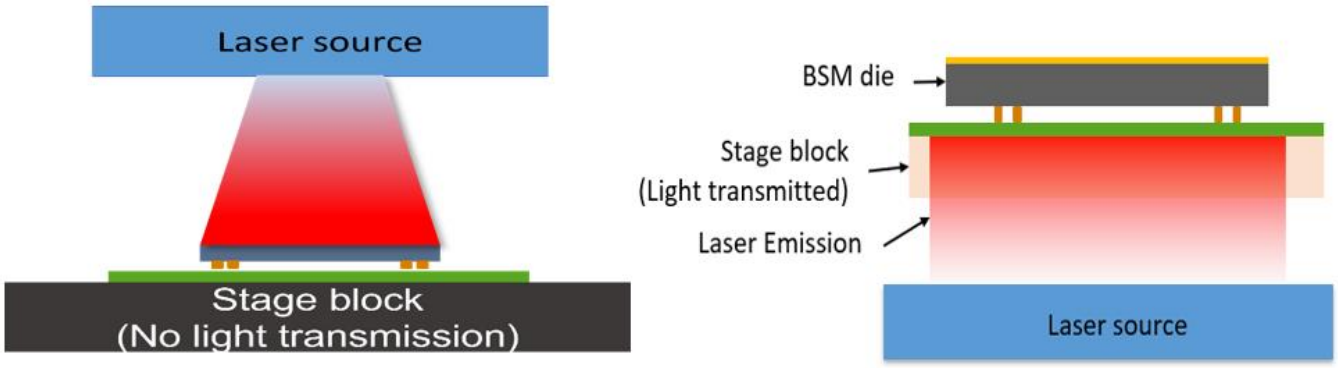
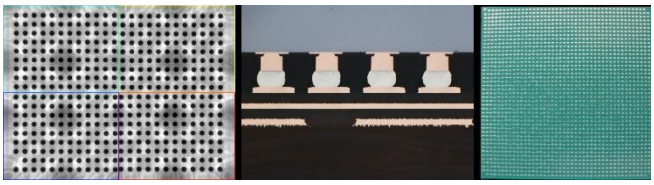


Figure 5. Schematic image of existing LAB (left) and Next Gen LAB (Reverse LAB) (right)

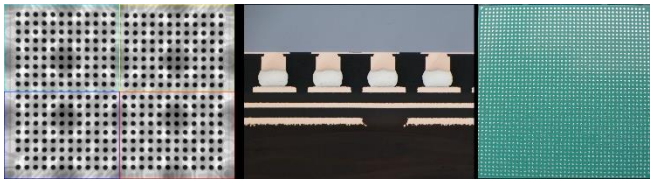
Results with Next Gen LAB

After a couple of trials adjusting power and time, optimum LAB conditions were achieved. With these POR conditions, the LAB parameter margin was investigated by applying ±10% of power. Fig. 6 shows the results. All three parameters show good interconnection without any bump non-wet, bump short or substrate surface damage at the BGA side.

POR condition.



POR-10% condition.



POR+10% condition.

Figure 6. X-ray and X-section and substrate visual inspection image with Next Gen LAB

Next, measurements were made of the peak temperature of the BSM die surface. Typically for LAB, an IR camera is used to measure temperature but for BSM die, temperature of bump area was also measured by a thermocouple (TC) because BSM surface temperature was expected to be low due to high reflectance. The thermocouple was inserted between the die and substrate at both die corner and die center positions as shown in Fig. 8. The IR peak temperature of the BSM die is only around 65~75°C due to the low emissivity of the metal. The substrate temperature is around 254~264°C at POR conditions. However, thermocouple temperature at the bump is around 254~259°C which exceeds the solder melting temperature. The IR peak image, IR temperature and thermocouple profiles are shown in Fig. 7 and Fig. 8, respectively.

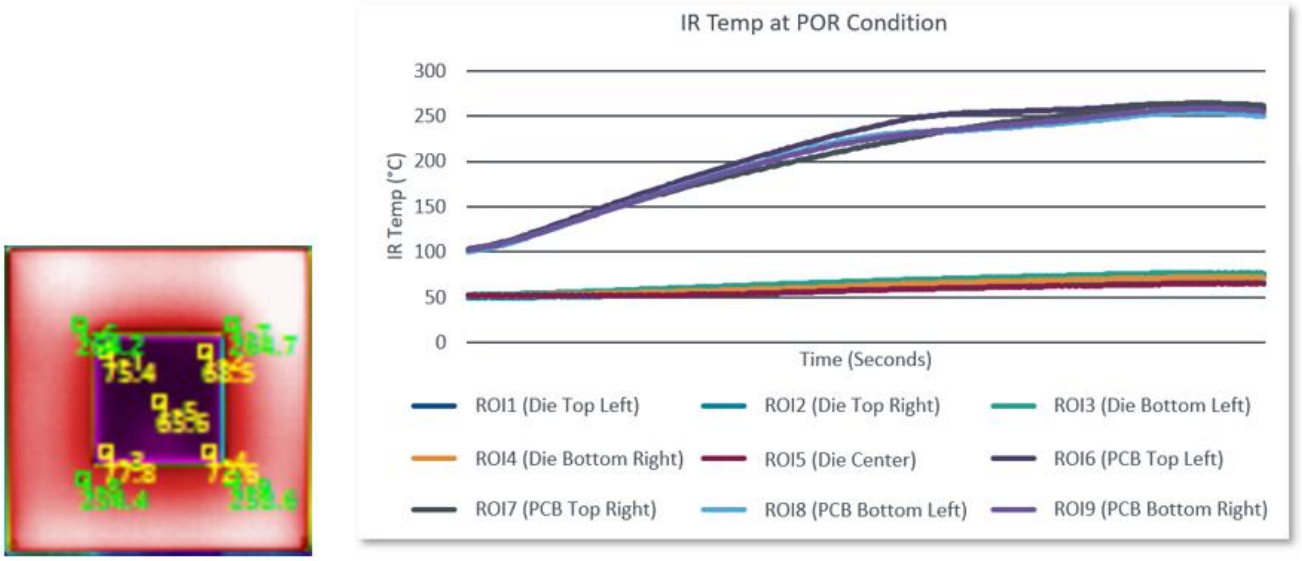


Figure 7. IR peak image (left) and IR profiles (right).

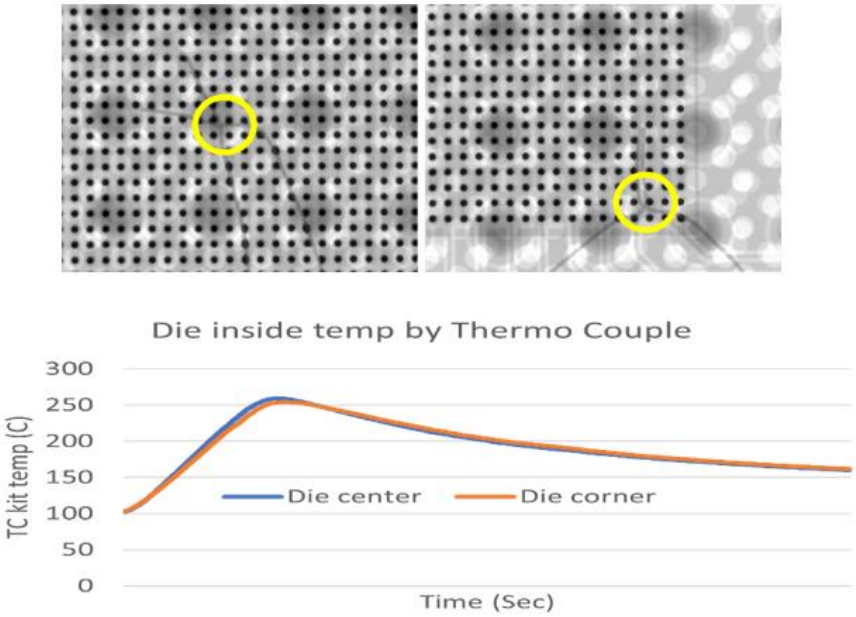


Figure 8. TC kit position (circles at top) and temperature profile (bottom).

Result with Mass Reflow

Mass reflow is possible because the bump pitch 165 µm is within the MR capability of 120 µm. Parts were assembled using standard reflow profiles for leadfree solders. As a result, there were no bump shorts in X-ray inspection and cross-section analysis as shown in Fig. 9. However, MR shows more solder side wall creep (wicking) than LAB and it is expected that MR will be difficult to apply for fine bump pitch devices. In other words, for high productivity, Next Gen LAB might be the only solution for fine bump pitch device with BSM die.

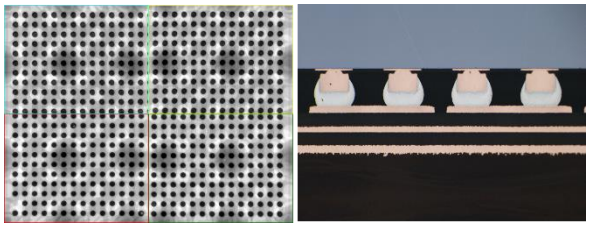


Figure 9. X-ray and bump X-section image with MR

Next Gen LAB Expandability

In addition to the BSM die application, DRAM attach and 2.5D module attach will need Next Gen LAB technology. Development continues for both applications and, to date, has achieved promising results with good interconnections. Table 4 shows the schematic image of the Next Gen LAB applications.

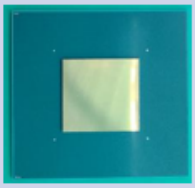
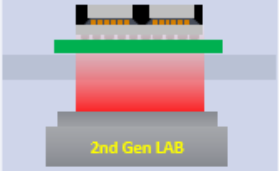
	BSM SOC	DRAM	2.5D module
Application for Next Gen LAB			

Table 4. Schematic image of Next Gen LAB applications.

Reliability Test

Parts were built with POR LAB conditions and subjected to standard JEDEC reliability tests. Ignoring lid and solder ball attach, the testing focused on bump interconnection to see if whether there were any post-reliability abnormalities. At each reading, SAT and bump cross section was checked. Unfortunately, Open/Short (O/S) testing was not performed due to O/S test socket unavailability. Finally, all reading points showed no SAT abnormalities and no abnormalities appeared in bump cross section through Unbiased Highly Accelerated Stress Test (UHAST)

192 hrs., Temperature Cycle, Condition B (TCB) 1000X and high temperature storage (HTS) 1000 hrs. as shown in Table 5.

Test Item	Test Conditions	Underfill SAT	Bump interconnection
MRT (L3)	-30°C/60% RH, 192hrs 3X 260°C reflow	27/27 (100%)	No abnormality
TCB	-55°C/125°C, 500X	13/13 (100%)	No abnormality
	-55°C/125°C, 1,000X	12/12 (100%)	No abnormality
HTS	150°C, 500 hrs	13/13 (100%)	No abnormality
	150°C, 1,000hrs	12/12 (100%)	No abnormality
HAST	130°C/85% RH, 96hrs	13/13 (100%)	No abnormality
	130°C/85% RH, 192hrs	12/12 (100%)	No abnormality

Table 5. Reliability test results.

Summary

This study demonstrated the viability of bump interconnection of BSM die using LAB technology. Due to the high reflectance of Au metallization of BSM at LAB, normal LAB conditions are not feasible due to lack of heat transfer to the bumps. Even though the LAB power was increased 4X or the LAB time was 16X longer, substrate surface damage or bump non wetting was detected. The conclusion is that it is very hard to optimize the LAB conditions and the process margin is very narrow. Existing Top LAB is not recommended for BSM die interconnections.

To improve quality, Next Gen LAB was developed. This is a reverse-type LAB where laser emission from bottom BGA side to bump is transmitted through stage vacuum block. The new LAB process shows promising results without observing substrate BGA side surface damage, bump non-wetting and bump shorts for the 165-µm bump pitch test vehicles. Also, ±10% parameter windows show no abnormalities as well. Parts built with POR LAB conditions show no abnormalities on SAT and the bump interconnections passed all JEDEC reliability tests through UHAST 192 hrs., HTS 1000 hrs. and TCB 1000X.

Mass reflow shows promising results as well for the 165-µm bump pitch test vehicle without observing bump short and bump non-wetting. However, MR shows more solder side wall creep (wicking) than LAB and it will be difficult to apply for fine bump pitch devices.

Next Gen LAB was developed to overcome the limitation of existing LAB and it might be the only solution for fine bump pitch interconnection of BSM die. This will also provide a solution for high bandwidth memory bonding and 2.5D module interconnection.

Additional Authors

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Acknowledgement

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Summary

[1] Sean S. Toom, et al., “Indium Thermal Interface Material Development for Microprocessors,” 2009 IEEE 25th SEMI-THERM Symposium, 2009.

[2] YunAh Kim, et al., “Metal Thermal Interface Material for Next Generation FCBGA,” 2021 Electronic Components and Technology Conference, 2021.

[3] MinHo Gim, et al., “High Performance Flip-Chip Bonding Mechanism Study with Laser Assisted Bonding,” 2020 Electronic Components and Technology Conference, 2020.