Wafer Dicing with TLS Technology

Improving Si and SiC Wafer Dicing Yields with Thermal Laser Separation

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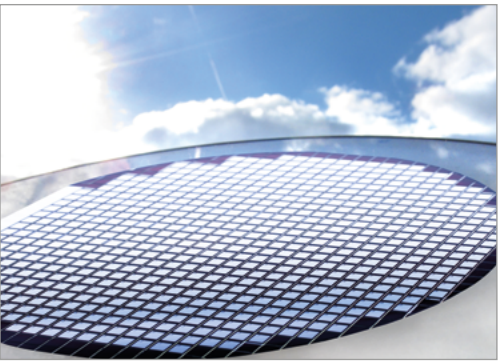

Increasing semiconductor content in mobile, high-performance computing, automotive and Internet of Things applications is driving continued growth in demand for materials such as silicon and silicon carbide (SiC). Silicon wafer shipments are expected to continue to reach record new levels through 2021 [1] while the SiC power device market is expected to grow from $302 million in 2017 to $1.5 billion in 2023.[2] For both silicon and SiC-based devices, die singulation – dicing the product wafers into individual dies that are subsequently packaged – is an essential process that is critical to product yields. At this stage, there is no possibility for rework, and maintaining the integrity and performance characteristics of the devices is paramount to fab profitability. Mechanical blade dicing is the predominant dicing technology in the semiconductor industry today for both silicon and SiC die singulation. However, with the migration to larger-sized substrates and thinner wafers, such as for 3D-IC packaging or for reducing on-resistance in vertical power transistors, mechanical blade dicing is increasingly challenged by cost of ownership, throughput and yield factors.

In a previous article [3], we investigated the yield benefits of applying a novel laser dicing approach, known as *TLS-Dicing*® (thermal laser separation), to SiC wafers, and demonstrated improved process performance by reducing or eliminating micro cracks, chipping and delamination that lead to yield loss. In this article, we will study the impact of thermal laser separation on the electrical performance of singulated SiC devices, which is a particularly crucial metric for power devices. In addition, we will also investigate the effects of thermal laser separation on wafer bending strength for both SiC and silicon wafers, a crucial parameter for wafer thinning applications.

Thermal Laser Separation (TLS)

TLS is a kerf-free laser-based dicing technology. [4] By performing TLS, a crack is guided by controlled thermally induced mechanical stress using a continuous-wave laser to locally heat up the material to be cut along the dicing street. Directly after the laser heated zone, a water aerosol quickly cools down the material (Fig. 1). This temperature gradient introduces a tensile stress capable of running one controlled crack independent of the lattice plane through the material. This cleaving process results in high edge quality without scratches, micro cracks or chipping, and runs with up to 400 mm/s feed rate. The complete wafer material is fully separated by one laser pass.

This cleaving is the main principle of TLS. Nevertheless, TLS is always a two-step process. The introduced stress field is capable of guiding a crack but not introducing a crack. Therefore, a crack must be introduced before the cleaving process. This is done by a scribing process where an initial crack is introduced in the material to be cut. This Initial Scribe involves a very short (less than 300 µm long) ablative laser scribe that is introduced at the beginning of the crack. TLS with Initial Scribe is used in the photovoltaic industry to cut solar cells into two half cells for half-cell modules. In order to increase the straightness of the TLS cleaving line, a *Continuous Scribe* can be used. With this technology a scribe is performed all along the line to be cut in order to define the cleaving position at each point along the cleaving line.

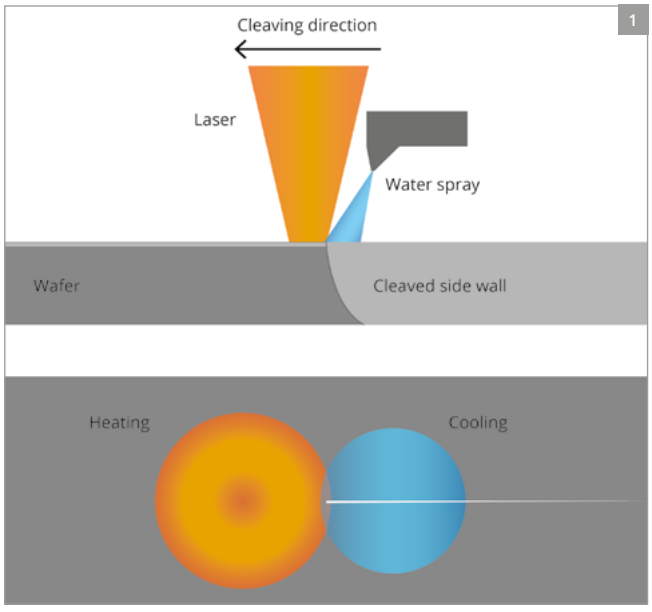

Fig. 1: Principle of TLS-Dicing®

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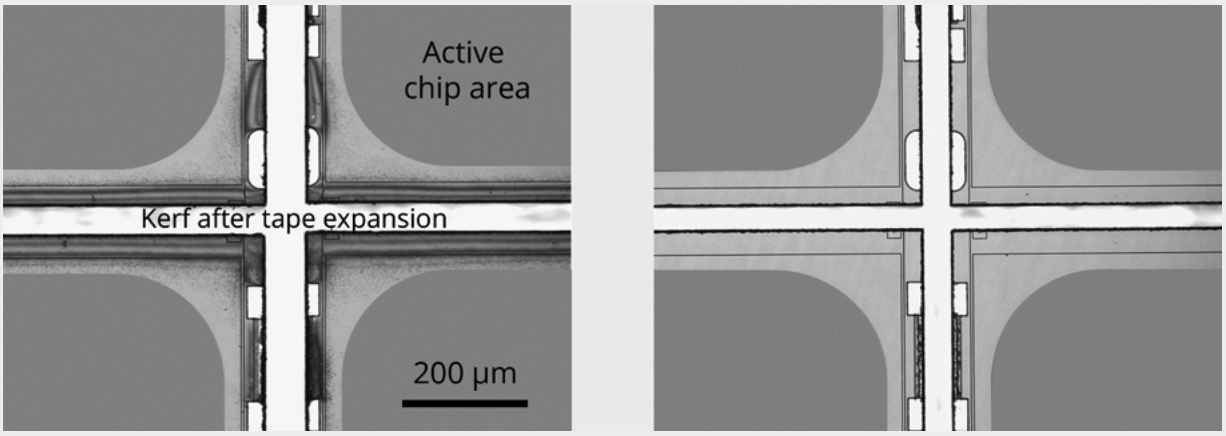


Fig. 2: Difference between standard surface scribe (left) and Clean Scribe (right). Structures inside dicing street are test structures. Tape was expanded after TLS dicing in order to visualize the kerf. Scribing depth for both scribes is approx. 20 µm.

For surface scribes on wafer substrates, two technologies are used. For SiC wafers, a continuous surface scribe together with a technology to remove particles in situ, called *Clean Scribe*, can be used. For silicon wafers, there are higher requirements regarding particles and breaking strength. Therefore, a different Continuous Scribe is needed for silicon, which is performed beneath the surface in order to not affect edges of the dice to be cut. This technology is called *Deep Scribe*. Following, these two different approaches for SiC and Si are explained in detail and results are shown.

TLS with Clean Scribe for SiC wafers

SiC is mainly used for power electronic devices. Main drivers for SiC wafer dicing are the dicing costs and the throughput. While mechanical blade dicing is sufficient for standard power electronic devices on silicon-based devices, this technology suffers from high process costs and low throughput with SiC dicing. This is due to the very high hardness and brittleness of SiC. However, these material properties make SiC an optimal candidate for the TLS technology. For example, the TLS feed rates of up to 400 mm/s are up to 40 times faster compared to mechanical blade dicing.

To improve straightness during TLS processing, a continuous surface scribe is used for TLS. Additionally, this surface scribe opens structures (e.g. product control monitoring structures) inside the dicing street or metal pads at the wafer edge region. Nevertheless, with a continuous surface scribe, particles are generated, which can subsequently migrate to the active chip regions and lead to yield loss during packaging. To minimize the number of particles without the need of expensive protective coatings, the Clean Scribe technology (patent pending) was developed. During Clean Scribe, a water aerosol (similar to the water aerosol used during cleaving) is applied to the laser influence zone. This water aerosol cools and removes the particles during their formation. In Fig. 2, two examples of a dicing street after scribing and cleaving are shown; one without and one with Clean Scribe technology. As shown in Fig. 2, Clean Scribe removed virtually all particles from the dicing street.

As demonstrated, TLS with the Clean Scribe technology is ideal to cut SiC wafers with thicknesses from 100 µm to 550 µm with one scribing path and one cleaving path with higher feed rates and higher edge quality compared to other dicing technologies. [5] In order to test the compatibility of the TLS process with the standard assembly workflow, fully processed SiC wafers were diced using TLS. After dicing, the wafers were inspected and assembled at a standard production line in an assembly fab.

These assembled devices were electrically analyzed for forward blocking characteristic as well as electrically/thermally stressed using a high temperature reverse bias (HTRB) test (Fig. 3). All electrical test results met specifications, proving good electrical performance of the TLS-diced chips. In addition to the electrical measurements, cross section analyses of the die attach were performed in order to prove the correct die attach on the lead frame. [6]

These results demonstrate that the electrical properties of the SiC diodes are not affected by the TLS process and it is possible

Wafer Dicing with TLS Technology

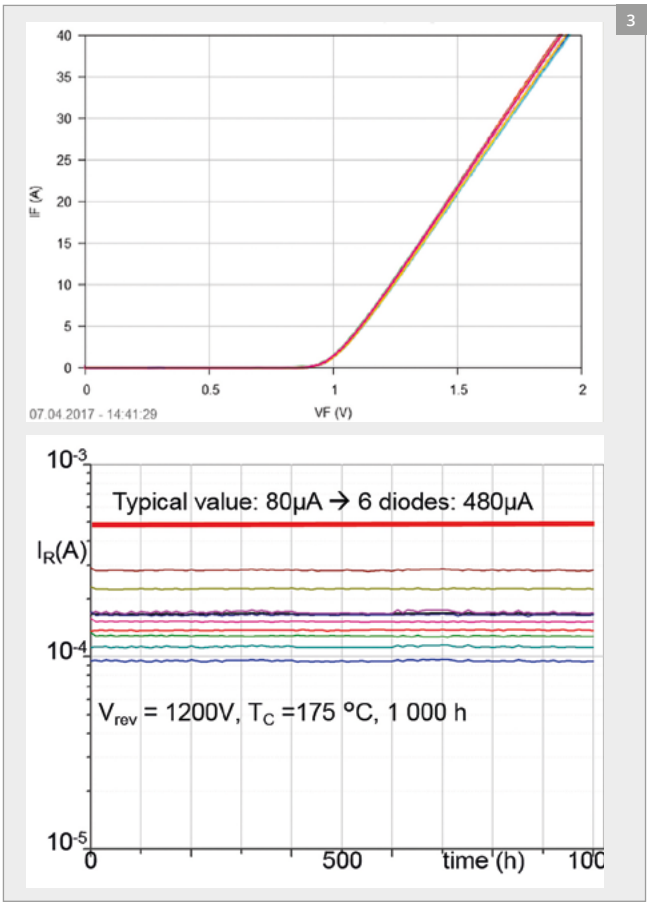


Fig. 3: Electrical characteristics of TLS diced and fully assembled SiC devices. Left: Forward I-V characteristics of 25 random samples of SiC diodes. Right: Reverse current IR during HTRB test (56 TLS-diced SiC diodes and 4 mechanical diced) [6]

to handle the zero kerf devices on the wafers for shipping and packaging in a high-volume backend facility.

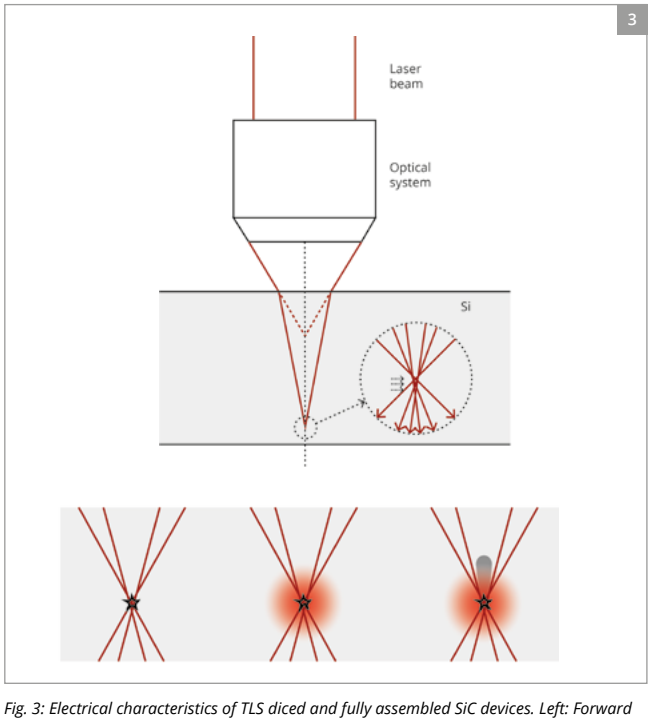
TLS with Deep Scribe for silicon devices

In order to improve the straightness and the bending strength of separated chips from silicon wafers, Deep Scribe technology was used. Deep Scribe is a laser-induced sub-surface material modification. A pulsed laser beam of near infrared wavelength is focused with an objective into the silicon, which is partly transparent at 1064 nm. Due to the refractive index, an extension of focal length and spherical aberrations will occur. Therefore, an optical system with a high numerical aperture and a capability to correct these spherical aberrations is used. The incident rays propagate through the silicon until the absorption increases abruptly when reaching the threshold fluence near the focal point. This increase in absorption results from the presence of free charge carriers and causes an increase in the temperature, which also causes lattice absorption to take place. Due to the heat conduction, a club shaped material modification along the caustic of the laser beam will be created (Fig. 4).

Compared to processes like stealth dicing, using the Deep Scribe technique modifies the material in only a very limited region. By adjusting parameters such as focus position, duration of laser pulse and laser power, an adjustment of the position and size of the modified area can be achieved. In combination with cleave, one single Deep Scribe layer is sufficient to separate a wafer up to 775 µm in thickness. Nevertheless, a stacking of two or more Deep Scribe layers is also possible in order to provide higher perpendicularity at the edges of the separated chips (Fig. 4).

If maximum bending strength is required, placing the Deep Scribe layer in the middle of the chip side wall will minimize the introduction of tensile stress to the modification layer during the bending test. To determine the bending strength of the separated dies, 200 µm thick wafers were cut with Deep Scribe TLS with layers on different layer positions. For comparison, similar wafers were cut with current state-of-the-art mechanical blade dicing. The chip size for this experiment was 3.6 x 3.6 sq. mm.

Breaking strength measurements were performed with a three-point bending test of 100 chips per side (front and back) for the



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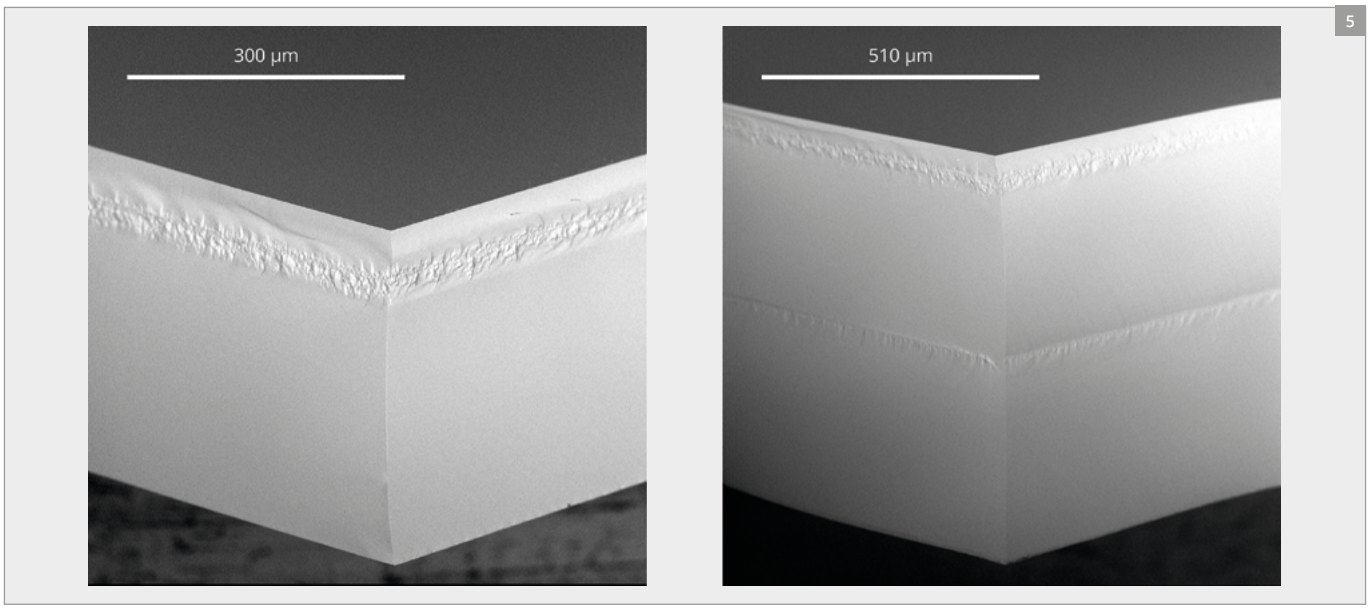

Fig. 5: SEM images of Si chips cut with Deep Scribe TLS. Left: 380 µm thick wafer with one Deep Scribe Layer. Right: 750 µm thick wafer with two Deep Scribe Layers

different dicing technologies. The evaluation was done by Weibull analysis distribution, whereby the values for the probability of breakage of 63.21% of all chips are determined. As expected, the breaking forces are maximized by moving the Deep Scribe layer into the neutral fiber (middle of the wafer), where the forces of front and back sides are nearly identical. With this approach, it is possible to achieve a more than three times higher stability of the separated chips than in the sawing process (Fig. 6).

Summary

Wafer dicing is an essential semiconductor fabrication process that is critical to die yields. As substrate sizes for SiC wafers scale upward, and new applications such as 3D/stacked die packages impact silicon wafer thickness, mainstream wafer dicing methods such as mechanical saw dicing become increasingly limited in their practical use. Thermal Laser Separation is a novel wafer dicing method that provides important cost-of-ownership, throughput and yield benefits for SiC and silicon wafers. As demonstrated in this article, the two-step TLS-Dicing® method eliminates the need for protective coatings to mitigate particle generation during the dicing process, provides dramatically improved breaking strength of processed wafers, and does not affect the electrical properties of processed die.

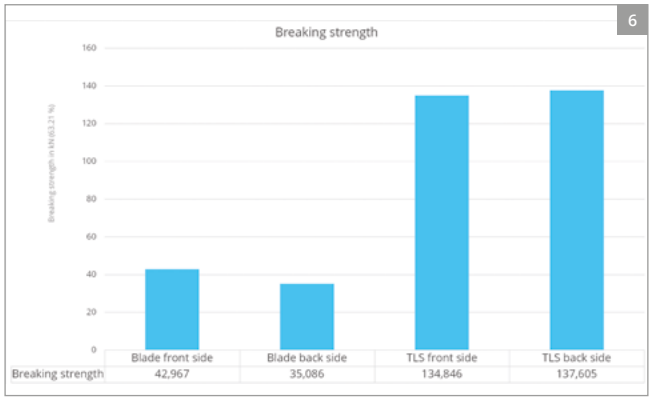

Fig. 6: Breaking strength evaluation of 200 µm thick Si wafers with 3.6 x 3.6 sq. mm chip size.

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