Free Webinar:

Contemporary Design for Testability Guidelines for Circuit Boards and Systems

December 10, 2014
8:00 - 9:00 a.m. PST

Presented in collaboration with A.T.E. Solutions

Abstract

Design for testability (DFT) and built-in self-test (BIST) have been widely adopted for ICs and have received broad support from designers and managers. New DFT standards and guidelines, such the 2014 SMTA/TMAG Testability Guidelines for board and system manufacturers, will be discussed. The concepts of boundary scan and BIST are briefly introduced and some relevant guidelines highlighted. When DFT and BIST are properly applied, the result is substantially better tests at lower costs. The weak link between test and design engineers can be overcome by successfully managing the DFT process, with better and more timely communication between the disciplines. The webinar will provide anecdotal evidence that DFT
Guidelines included early in the design process provide the most cost-effective way to profit from such guidelines. The webinar will conclude with some “futuristic” testability techniques that will not only keep up with contemporary advances in technology, but can actually exploit under test (UUT) intelligence towards less costly and more comprehensive tests.

Ridgetop Group and Advanced Test Engineering (A.T.E.) Solutions, Inc. invite you to attend a one-hour webinar to learn about DFT guidelines and how to effectively manage them. Whether you are totally technical or mainly management, you will find the topic useful and the time well spent.

Learning Objectives

- Learn to identify, utilize, evaluate and manage DFT guidelines available commercially.
- Learn how boundary scan-related standards and BIST have changed the testability paradigm.
- Learn how to overcome traditional obstacles to creating testable designs.
- Peek into the (possible) future of testability.

Speaker

Louis Y. Ungar is president of Advanced Test Engineering (A.T.E.) Solutions, Inc., a leading test and testability consultancy and educational firm. Having introduced the first university course on Automatic Testing and Design for Testability at UCLA, he and his company have taught similar courses to thousands around the world publicly held forums, at company facilities and online. He led the Surface Mount Technology Association (SMTA) Testability Committee to publish the 2014 SMTA/TMAG Testability Guidelines. He has been involved with the IEEE standards committee for several design for testability standards, including the IEEE-1149.1, the 1149.4 and the P1687. He has been honored as a lifetime member of the American Society of Test Engineers (ASTE). He is the founding president of the not-for-profit Testability Management Action Group (TMAG). He has completed courses towards an MA in management and holds a BS degree in Electronics Engineering and Computer Sciences from UCI. He holds patents in built-in self-test technology, has developed test engineering software such as The Testability Director, and is a highly sought-after speaker, instructor and consultant in all aspects of test, testability and BIST.

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