Imec, Holst Centre and Renesas Present World’s Lowest Power 2.4GHz Radio Chip for Bluetooth Low Energy

SAN FRANCISCO (ISSCC 2015, International Solid State Circuits Conference) – Feb. 24, 2015—Today, at the 2015 International Solid State Circuits Conference (ISSCC), Imec, Holst Centre and Renesas presented an ultra-low power 2.4GHz short range radio compliant with Bluetooth® Low Energy (BLE) and IEEE802.15.4 (ZigBee). Implemented in 40nm CMOS, the radio achieves a reduced supply voltage (20 percent), power consumption (25 percent), and chip area (35 percent), as compared to the previous 90nm RF front-end design.

“From healthcare to smart buildings, ubiquitous wireless sensors connected through cellular devices are becoming widely used in everyday life,” said Harmke De Groot, Department Director at imec. “The radio consumes the majority of the power of the total system and is one of the most critical components to enable these emerging applications. Moreover, a low-cost area-efficient radio design is an important catalyst for developing small sensor applications, seamlessly integrated into the environment. Implementing an ultralow power radio will increase the autonomy of the sensor device, increase its quality, functionality and performance and enable the reduction of the battery size, resulting in a smaller device, which in case of wearable systems, adds to user’s comfort.”

Imec, Holst Centre and Renesas’ new 2.4GHz radio achieves world-class energy efficiency by employing a digital-intensive RF architecture tightly integrated with the digital baseband (DBB) and a microcontroller (MCU). Additionally, several low-voltage techniques are adopted to ensure sub-1V operation, achieving best-in-class 3.7mW RX and 4.4mW TX power consumption. Furthermore, the digital-intensive RF design reduces the analog core area to 1.3mm², and the DBB/MCU/SRAM occupies an area of 1.1mm².

Fabricated in a 40nm CMOS process, the radio supports the most common standards for mobile sensor networks (BLE, IEEE802.15.4). A mixed-mode fast Carrier Frequency Offset (CFO) compensation through a 2-point injection All-Digital Phase-Locked Loop (AD-PLL) expands the receiver’s tolerance to Carrier Frequency Offset (CFO) from ±20ppm to ±60ppm. An All-Digital PLL is used because of its small area and extensive self-calibration. An excellent receiver (RX) sensitivity of -93.5dBm (BLE spec.: <-70dBm) for BLE was measured, with a packet error rate (PER) of 30.8 percent. The RX with fast Automatic Gain Control (AGC) has a dynamic range from the sensitivity level up to -5dBm (BLE spec.: >-10dBm), and fulfills BLE requirement on adjacent channel rejection with sufficient margin.
Ultra-low power multi-standard 2.4 GHz radio compliant with Bluetooth Low Energy and ZigBee

This press release