“Embedded wafer-level-package activity is expected to pick-up by 2015 above $200M,” says Yole Développement

“FOWLP & Embedded Die Packages”, a report from Yole Développement

Lyon, France – November 7, 2012: Yole Développement announces its FOWLP & Embedded Die Packages report. In this report, Yole Développement offers an analysis of both FOWLP and Embedded die package technologies detailing key market drivers, benefits and challenges application by application, technology roadmaps and manufacturing tool-box, supply chain perspectives, key players and emerging infrastructure for Embedded WLP. A package cost structure analysis based on real products available on the market completes the analysis.

FOWLP technology is looking for new driving forces beyond Intel mobile’s push

After Infineon’s strong push for eWLB technology commercialization and the resulting surge in growth, the FOWLP market reached the $100M market last year. Revenue is now stabilizing as Intel Mobile will phase out progressively their key wireless baseband SoC product production, outsourced currently at packaging subcontractors ASE (TW), NANIUM (PT) and STATS ChipPAC (SG).

“This young industry will need to wait until 2015 – 2016 to reach $200M, as the demand will shift from IDMs to leading fab-less wireless IC players, such as Qualcomm, Broadcom, Mediatek, etc… and will be supported by the solid infrastructure of ‘top 4’ major assembly houses,” explains Lionel Cadix, Market & Technology Analyst, Advanced Packaging at Yole Développement.

Low reliability on large package body size and lack of flexibility in the IC to package co-design process are the two main factors limiting the wide adoption of FOWLP technology on the wireless IC market. Indeed, FOWLP technology imposes a specific redesign of the chip for efficient integration into the package: both Infineon and STEricsson (who already have products on the market) spent almost 18 month to redesign their baseband and RF-Transceiver SoCs in order to place the pads at optimized locations and match with a single RDL, 0.5mm board pitch eWLB package design. FOWLP is a restrictive package technology for most of the world’s IC designers to adopt efficiently, especially fabless chip companies. This is why only big semiconductor IDM companies having IC-to-package co-design environments well established in-house can drive and support the initial growth of this new wafer-level-packaging platform at its early stages.

Two main OSATs supporting FOWLP infrastructure today. Four more players to come next!

FOWLP is clearly the “Middle-end” platform of choice for packaging assembly & test ‘OSAT’ suppliers of the IC industry, as all implies a simplification and consolidation of the entire packaging, assembly & test and supply chain inside one single factory.

NANIUM (PT) and STATS ChipPAC (SG) shared more than 80% of the $107M FOWLP activity revenue last year, mainly driven by Intel Mobile’s volume demand on eWLB production. While ASE (TW) is shutting down its 200mm eWLB operations this year to focus on future generation FOWLP technologies, many OSAT players are presently in qualification phase such as ADL (TW), Amkor (KR) and NEPES (SG). Additional packaging houses are expected to come onboard in the 2013 – 2014 timeframe such as TSMC (TW), SPIP (TW) and J-Devices (JP). More details on the supply chain challenge and the partnership already in place are provided in this research report update.
Embedded die package platform successfully entered the SiP module business

Meanwhile, the embedded die in package industry has taken a giant step forward in 2011 since AT&S (AT) and TI (US) started the commercialization of microSiP DC/DC converter modules with critical mass volume, production of >100M units this year, driven by the mobile market. Rohm (JP) and Epco-TDK (JP) would be the second source of the same microSiP power conversion module in the mobile handset supply chain of RIM (CA). IC substrate suppliers Taiyo-Yuden (JP) and Fujikura (JP) are also getting ready to ramp-up their internal assembly lines for embedded die packaging. This will bring the total number of players to 4 in the near future, with separate supply chains able to support the embedded die in package technology commercialization.

Today, main roadblocks for embedded die package commercialization are mainly linked to low manufacturing yields (75-85% overall) and supply chain settlement issues in both the embedded die wafer preparation as well as in back-end assembly & test operations. Again, only a large semiconductor IDM company such as Texas Instruments (US) could successfully lead the commercialization of this new packaging assembly platform by filling the gaps (in terms of investment, risk and know-how) and settle the supply chain.

The most pragmatic approach to commercialize embedded die package technology will be to initially start with simple, low cost, low I/Os, small die analog & power IC applications (such as DC/DC converter modules, IPD networks, RFID, Power MOSFET, IGBT modules, auto-focus driver ICs, etc...).

Embedded die packaging is supported by a game changing, low cost, panel area, PCB based infrastructure that has the potential to create a new space, an alternative supply chain for today’s well established package standards such as QFN/SOT/WLCSP/BGA platforms. Being intrinsically “3D” capable, the technology is well positioned to meet the future requirements of miniaturized, low cost 3D SiP module configurations.

“Today, first generations of FOWLP and embedded die package technologies are not really competing as they are driven by different players and will initially target very different application...
spaces. However, this situation is likely to change radically in the near future as “2nd generation
derivatives of both platforms appear on the market,” adds Jérôme Baron, Business Unit Manager,
Advanced Packaging at Yole Développement.

About FOWLP & Embedded Die Packages report:

- Authors:
  Lionel Cadix joined Yole Développement after the completion of several projects linked to the
  characterization and modeling of high density TSV and 3DIC chip stacking in collaboration with CEA-
  Leti and STMicroelectronics during his PhD. He is author of several publications and 8 patents in the
  field of 3D Integration.
  Jerome Baron is leading the semiconductor packaging market research at Yole Développement. He
  has been following the 3D packaging market evolution since its early beginnings at device,
  equipment and material levels. He was granted a Master of Science degree from INSA-Lyon in
  France.

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  83 01 90).

- Companies cited in this report:
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market research, technology analysis, strategy consulting, media in addition to finance services. With a solid
focus on emerging applications using silicon and/or micro manufacturing, Yole Développement group has
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CONTACTS

For more information about:
• Services: Jean-Christophe Eloy (eloy@yole.fr)
• Reports: David Jourdan (jourdan@yole.fr)
• Media: Sandrine Leroy (leroy@yole.fr)

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