International Wafer-Level Packaging Conference Press Release

For more info contact:
Jenny Ng
952-920-7682
jenny@smta.org

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International Wafer-Level Packaging Conference (IWLPC) Workshops

Minneapolis, MN - The SMTA and *Chip Scale Review magazine* are pleased to announce the Workshops for the 13th Annual International Wafer-Level Packaging Conference (IWLPC). On Thursday, October 20, there will be professional workshops given by instructors who are pre-eminent authorities in their fields. IWLPC will be held October 18-20, 2016 at the DoubleTree Airport Hotel in San Jose, California.

WS1: Introduction to Fan-Out Wafer-Level Packaging
Beth Keser, Ph.D., Qualcomm
8:30am-12:00pm

Fan-Out Wafer-Level Packaging (FO-WLP) technologies have been developed across the industry over the past 15 years and have been in high volume manufacturing for over 8 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wirebond and bump interconnections, substrates, leadframes, and the traditional flip chip or wirebond chip attach and underfill assembly technologies across multiple applications. This course will cover the advantages of FO-WLP, potential application spaces, package structures available in the industry, process flows, material challenges, design rule roadmap, reliability, and benchmarking. This course has been updated with over 10% new material compared to the first time it was offered last year at IWLPC.

WS2: Wafer-Level Packaging for the Functional Integration of MEMS and ICS
Chip Spangler, Ph.D., Aspen Microsystems, LLC
8:30am-12:00pm

The development of Wafer-Level Packaging (WLP) has been a major driving force for the size and cost reduction for integrated circuits as well as MEMS, microsystems, micro-optical and microfluidic products. Collectively referred to as MEMS, these devices require highly specialized packages that protect the fragile microstructures and still allow the desired signals, both electric and non-electric, to pass through the package to the die. The challenges and costs associated with MEMS packaging has, since the 1970's, driven the development of Wafer-Level Packaging and associated technologies such as silicon and glass interposers, through wafer vias, wafer bonding and die stacking. Cost and size demands have since lead to the widespread adaptation of these MEMS-based WLP technologies by the integrated circuit package community. More recently the demand for multi-sensor products, greater levels of sensor intelligence and the connectivity requirements of IoT applications has driven the complex integration of MEMS and ICs through the use of WLP technologies.

WS3: Choosing the Right IC Packaging
Chet Palesko, SavanSys Solutions LLC and Jan Vardaman, TechSearch International, Inc.
1:30pm-5:00pm

In this course, we will analyze the performance and size characteristics of traditional (lead frame options, wire bond PBGA, flip chip PBGA) and advanced packaging (Wafer-Level Packaging, Fan-Out WLP options, embedded die, 2.5D/interposer-based packaging, 3D packaging with through silicon vias). For each packaging technology, this course also provides a detailed cost analysis including the manufacturing process flow to fabricate and assemble the package and the dominant technology cost drivers.
This course will also examine how OEMs and suppliers can collaborate to develop a model which optimizes product manufacturing cost for IC packages. This modeling approach has been successfully used by a number of major OEMs and suppliers in North America, Europe, and Asia to match design technology choices with supplier competencies. Yields are improved and cost reduction is achieved across the entire supply chain.

WS4: Recent Advances and New Trends in Semiconductor Packaging
John Lau, Ph.D., ASM Pacific Technology
1:30pm-5:00pm

Recent advances in, e.g., Fan-Out Wafer/Panel Level Packaging (TSMC's InFO-WLP and IZM's FO-PLP), 3D IC packaging (TSMC's InFO_PoP vs. Samsung's ePoP), through-silicon vias (TSVs), microbumps, 3D IC integration (Hynix/Samsung's HBM for AMD/NVIDIA's GPU vs. Micron's HMC for Intel's Knights Landing CPU), 2.5D IC Integration (TSV-less interconnects and interposers), embedded 3D hybrid integration (of VCSEL, driver, serializer, polymer waveguide, etc.), 3D CIS/IC integration, 3D MEMS/IC integration, thin-wafer Handling, thermal management, semiconductor and packaging for IoTs are examined, and their new trends will be discussed in this lecture. The patents impacting the semiconductor packaging the most (so far) will be mentioned first and the patent issues of Fan-Out Wafer/Panel-Level will be discussed and some recommendations will be made.

Visit www.iwlpc.com for more information.
Contact Jenny Ng at 952-920-7682 or jenny@smta.org with questions.

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