A New Development of Thermally Enhanced GaN-QFN with Heat Slug Attach Bonding Technology
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Abstract
GaN mosfet provides significantly lower resistance and low capacitance than silicon mosfet which makes GaN mosfet considered as alternative power devices to replace silicon mosfet, and by the adoption of GaN mosfet technology, the high-frequency power supply can be designed in small form factor by miniaturization of passive components. Integrated architecture with driver IC and GaN mosfet in QFN-SIP (System in package) is preferred solution to maximize the electrical performance of GaN devices, but this QFN-SIP has its own thermal challenge as it contains driver IC power dissipation and GaN mosfet power dissipation in one package so thermal improvement solution of QFN-SIP is required to be used in power supply without having thermal problems.

In this paper, various thermal improvement methods are recommended about 8x8mm QFN-SIP available in the market now, simulation study compares maximum junction temperatures and thermal resistance of QFN-SIP by increasing package size, increasing leadframe thickness, changing die location, and Cu clip bonding and Ag sintering attach.

Thick leadframe QFN-SIP can be achieved by heat slug bonding technology, and QFN 10x12mm with heat slug bonding samples build completed to run MSL3 3x reflow and temperature cycle and power cycle test.

I. Introduction
GaN mosfet has gained interest for power electronics and high-frequency application due to its improved semiconductor properties compared to silicon mosfet. GaN mosfet has significantly lower resistance and capacitance which can reduce conduction loss and switching loss in power system. Traditionally GaN mosfet is packaged as a discrete device and driven with separate driver IC due to different package requirement. However, the discrete package approach aggravates electrical performance due to significant package, and PCB interconnects parasitic power loops as have been demonstrated by multiple studies.[1-5]

Discrete GaN mosfets are packaged in various types such as through-hole package or leaded surface mount package or leadless DFN or QFN package. All of these packages have excellent thermal performance to handle high power dissipation on GaN mosfet.

In terms of electrical performance, integrated QFN-SIP architecture with driver and GaN mosfet is the best-optimized solution with minimum parasitic inductance in the package which enables high frequency power supply design possible. But this integrated QFN-SIP architecture creates thermal challenges as it includes driver IC and GaN mosfet heat dissipation on the same package. Integrated QFN SIP has many signal pins for Driver IC and fused pins for GaN mosfet connection which flow high current from GaN mosfet to circuit.

So ideal QFN-SIP should have thick fused leadframe which can handle high power dissipation from GaN mosfet and standard leadframe with many signal pins for driver IC features. In this paper, heat slug bonding on leadframe QFN-SIP concept is suggested and by using heat slug bonding technology, primary heat source GaN mosfet is attached on thick leadframe to improve the thermal performance.

II. GaN discrete package and QFN-SIP in the market
Typically discrete GaN mosfet is offered in various type of packages such as through-hole package or leaded surface mount type package or leadless QFN style packages to meet different power system requirement, and three popular discrete packages are shown in Fig. 1.

Power discrete packages like TO-247 and DSO-20 with thick leadframe usually includes large GaN dies inside packages to get lower resistance, and DFN types packages are used for high frequency DC-DC or AC-DC converter where lower package parasitic inductance value is also crucial in this application.

Fig. 1. Example of discrete GaN packages in the market
On the other hand, integrated driver IC and GaN mosfet in QFN-SIP is also available in the market shown in Fig 2. In this paper, QFN-SIP thermal performance improvement proposals are simulated and the effectiveness of each proposal will be discussed. Proposed thermal improvement methods are increasing body size and heat slug bonded leadframe and using cu clip bonding to replace wire bonding, and Ag sintering attach material instead of standard epoxy attach material.
III. QFN-SIP Simulation condition and modeling

The simulation used JEDEC still air chamber model shown in Fig. 3 and natural Convection as per JESD 51-2A with four-layer PCB, which has a size of 40mmx40mm and PCB metal layer structure is shown in Fig. 4.

Table 1. Bill of Material for simulation

<table>
<thead>
<tr>
<th>PKG</th>
<th>8x8 or 10x10 or 10x12</th>
<th>mm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN size</td>
<td>6x2.3</td>
<td>mm²</td>
</tr>
<tr>
<td>IC size</td>
<td>5.2 x 1.3</td>
<td>mm²</td>
</tr>
<tr>
<td>Leadframe thickness</td>
<td>0.2 or 0.5</td>
<td>mm</td>
</tr>
<tr>
<td>Heat slug thickness</td>
<td>none or 0.2 or 0.5</td>
<td>mm</td>
</tr>
<tr>
<td>GaN Power dissipation</td>
<td>8.5</td>
<td>Watt</td>
</tr>
<tr>
<td>Driver IC Power dissipation</td>
<td>0.5</td>
<td>Watt</td>
</tr>
<tr>
<td>Lead counts</td>
<td>33L (wire bond)/29L(Cu clip)</td>
<td></td>
</tr>
<tr>
<td>PCB size</td>
<td>40 x 40</td>
<td>mm²</td>
</tr>
<tr>
<td>PCB Cu pad layer</td>
<td>M1: 9.7x7.5, M2 &amp; M3: 40x40, M4: 30x30</td>
<td>mm²</td>
</tr>
</tbody>
</table>

Table 2. Thermal conductivity table

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Conductivity [W/mK]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mold compound</td>
<td>0.96</td>
</tr>
<tr>
<td>GaN Die</td>
<td>130</td>
</tr>
<tr>
<td>Silicon Die</td>
<td>117-0.42x(T-100)</td>
</tr>
<tr>
<td>Die attach Epoxy</td>
<td>4</td>
</tr>
<tr>
<td>Die attach Ag sintering</td>
<td>130</td>
</tr>
<tr>
<td>Leadframe type</td>
<td>C194</td>
</tr>
<tr>
<td>Heat slug bonding Ag sintering</td>
<td>130</td>
</tr>
</tbody>
</table>

IV. Simulation design of experiment

Bill of materials for simulation are shown in the table. 1 and JEDEC still air chamber model is shown in Fig. 3 and the ambient temperature is set as 50°C, thermal simulation has been performed with different optimization of QFN-SIP as below:

- Different package size
- Thicker leadframe by using heat slug bonding
- GaN mosfet attached location on leadframe
- GaN mosfet drain connection by wire bond or Cu clip bond
- Conventional epoxy attach material vs. Ag sintering attach material

Table 3. Leadframe die pad size and heat slug dimension

<table>
<thead>
<tr>
<th>Package</th>
<th>Die attach paddle size [mm]</th>
<th>Die pad area [mm²]</th>
</tr>
</thead>
<tbody>
<tr>
<td>8x8 QFN</td>
<td>3.75</td>
<td>6.2</td>
</tr>
<tr>
<td>10x10 QFN</td>
<td>8.85</td>
<td>6.7</td>
</tr>
<tr>
<td>10x12 QFN</td>
<td>10.85</td>
<td>6.7</td>
</tr>
<tr>
<td>Heat slug</td>
<td>7.2</td>
<td>4.8</td>
</tr>
</tbody>
</table>

Above fig. 5 described QFN-SIP package wireframe model which integrated driver IC and GaN mosfet on same leadframe and lead are separated from leadframe for GaN mosfet drain connection with either wire bonding or Cu clip bonding and multiple vias are located under leadframe area which can help to transfer the heat from driver IC and GaN mosfet to PCB efficiently.
In the simulation study, different size packages have different die attach paddle size described above Table 3. In principle, enlarge body size from QFN 8x8mm to QFN 10x10 mm or QFN 10x12mm which make die paddle size larger which helps heat transfer from the package to PCB easier. With 10x10 QFN and 10x12mm used the same heat slug size in below Table 3.

Comparison of vertical structure between regular leadframe QFN and heat slug bonding thicker leadframe QFN are shown below in Fig. 6, and the upper drawing shows regular leadframe QFN which integrated driver IC, and GaN mosfet dies on leadframe, and lower drawing of heat slug bonded on leadframe which integrated driver IC and GaN mosfet dies on heat slug bonding leadframe.

![Regular leadframe and heat slug bonded leadframe](image)

Fig. 6. Regular leadframe and heat slug bonded leadframe

Simulation study condition in Table 1, GaN mosfet is a primary heat source in QFN-SIP, so GaN location on leadframe is considered as one of the simulation options to analyze the thermal performance of the package. Therefore two different GaN mosfet locations options are considered in simulations (Fig. 7).

Most of GaN QFN-SIP with integrated driver IC and GaN mosfet has bottom location GaN attachment which can make GaN mosfet drain wire bonding shorter to achieve lower resistance and inductance in package, but thermal performance point of view bottom located GaN attach can limit heat transfer spread over entire leadframe and PCB so degrade thermal performance of QFN-SIP which lead to higher maximum junction temperature[Max Tj] as well as Rtheta-JA and Rtheta-HS as well.

As shown in Table 1, power dissipation is set 8.5watt for GaN and 0.5watt for driver IC and the ambient temp is set to 50°C.

Simulation result of different DOEs are shown in Table 4, and maximum Junction temperature[Max Tj] and thermal resistances are compared.

Option A simulation shows the improvement by increasing package size to 10x10mm QFN SIP, compared with Ref 8x8mm QFN SIP, Max Tj value is 212.4 °C which is 7.2 °C lower, and Rtheta-JA is 18.04[°C/W] and Rtheta-HS is 3.89[°C/W] which are 4.3% and 19.2% lower than thermal resistances of 8x8mm QFN-SIP.

Option B simulation shows the improvement by increasing package size to 10x10mm QFN SIP and adding heat slug bonding on leadframe to make total 0.4mm thick leadframe compared with ref 8x8mm QFN SIP, Max Tj value is 208.2 °C which is 11.4 °C lower, and Rtheta-JA is 17.58[°C/W] and Rtheta-HS is 3.89[°C/W] which are 6.7% and 30.9% lower than thermal resistances of 8x8mm QFN-SIP.

Option C simulation shows the improvement by increasing 10x10mm QFN SIP and using 0.4mm thick leadframe with heat slug bonding and changing the location of GaN mosfet in the center of leadframe compared with Ref 8x8mm QFN SIP Max Tj value is 201.2°C which is 18.4°C lower than Max Tj of 8x8 QFN SIP and Rtheta-JA is 16.8[°C/W] and Rtheta-HS is 2.63[°C/W] which are 10.8% and 45.3% lower than thermal resistances of 8x8mm QFN-SIP.

Only difference between option B and Option C is GaN die attach location and option C GaN mosfet is attached on center of leadframe, and option C reduces maximum junction temperature by 7°C, and RthetaJA and RthetaJ-HS are 16.8[°C/W] and Rtheta HS is 2.63[°C/W] which is 4.4% and 20.8% lower than Option B thermal resistance values.

Thermal resistance values with different options are summarized in the below graph (Fig.8.)
VI. Temperature profile analysis for 10x10 QFN-SIP

Further detail temperature profiles comparisons are made for option B and C and D which use same 10x10 QFN SIP and heat slug bonded 0.4mm leadframe.

In case of Option B, GaN mosfet drain is wire bonded to drain leads, and GaN mosfet is located on the bottom of leadframe, and GaN mosfet and driver IC are attached by epoxy attach material shown in table 2. In case of Option C, GaN mosfet drain is wire bonded to drain leads, and GaN mosfet is located in the center of leadframe, and GaN mosfet and driver IC are attached by epoxy attach material shown in table 2. In case of Option D, GaN mosfet drain is Cu clip bonded to drain leads, and GaN mosfet is located in the center of leadframe, and GaN mosfet and driver IC are attached by epoxy attach material shown in table 2.

Option B temperature profile of PCB and package surface and internal package are shown in below Fig. 9. Hottest temperature spot is GaN die location which is 208.2°C, and lowest temperature on PCB is simulated at 67.68°C, and the lowest temperature spot inside package is 184.4°C on leadframe. Leadframe temperature profile spread from 208.2°C to 184.4°C, so temperature difference is 23.8°C on the same leadframe.

Option C temperature simulation of PCB and package surface and internal package are shown in below Fig. 10 and hottest temperature spot is GaN die location which is 201.2°C and lowest temperature on PCB is 69.85°C, and the lowest temperature spot inside package is 186.1°C on leadframe and 181.1°C on drain pins and option D, GaN mosfet attach area, and leadframe temperature profile spread from 201.2°C to 185.8°C, so temperature difference is 14.7°C on same leadframe die attach paddle area.

Option D temperature simulation of PCB and package surface and internal package are shown in below Fig. 11 and hottest temperature spot is GaN die location which is 200.5°C and lowest temperature on PCB is 69.41°C, and lowest temperature spot inside package is 185.8°C on leadframe and 187.7°C on drain pins and option D, GaN mosfet attach area, and leadframe temperature profile spread from 200.5°C to 185.8°C, so temperature difference is 14.7°C on same leadframe die attach paddle area.

VII. Sample build for Heat slug bonding technology

To validate the concept of heat slug bonding on leadframe, QFN 10x12mm with GaN die was built with materials shown in below table 5.

<table>
<thead>
<tr>
<th>Table 5. QFN 10x12mm bill of materials</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
</tr>
<tr>
<td>GaN Die size</td>
</tr>
<tr>
<td>GaN Backside metal</td>
</tr>
<tr>
<td>Wire bond</td>
</tr>
<tr>
<td>Leadframe</td>
</tr>
<tr>
<td>Heat slug</td>
</tr>
<tr>
<td>Heat slug attach</td>
</tr>
<tr>
<td>GaN attach</td>
</tr>
</tbody>
</table>

QFN 10x12mm sample used same Ag sintering attach material for heat slug bonding and die attach process.
QFN 10x12mm sample wire bonding diagram is shown in Fig. 12.
Table 7. QFN 10x12mm vertical stack up dimension

<table>
<thead>
<tr>
<th>Material</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mold Cap</td>
<td>2 mm</td>
</tr>
<tr>
<td>GaN die</td>
<td>0.2 mm</td>
</tr>
<tr>
<td>Die Attach</td>
<td>0.03 mm</td>
</tr>
<tr>
<td>Heat slug thickness</td>
<td>0.25 mm</td>
</tr>
<tr>
<td>Heat slug attach</td>
<td>0.06 mm</td>
</tr>
<tr>
<td>Leadframe thickness</td>
<td>0.25 mm</td>
</tr>
<tr>
<td>Total package thickness</td>
<td>2.25 mm</td>
</tr>
</tbody>
</table>

Table 7 shows materials thickness of GaN 10x12mm QFN packages which uses 0.25mm thickness of Leadframe and 0.25mm thickness heat slug and 0.03mm Ag sintering attach thickness for GaN die attach and 0.06mm Ag sintering attach for heat slug bonding process.

Ag sintering dispensing pattern selection is a critical step to guarantee proper adhesion between heat slug and leadframe interface after multiple iterations of dispensing pattern above dispense pattern (Fig. 14) is selected which shows good coverage of Ag sintering attach surrounding heat slug as well as minimal void under heat slug.

Heat slug is bonded to leadframe sample photos shown in Fig. 15, which shows 100% coverage with good fillet four sides of heat slug without bleeding out.

Heat slug bonding on leadframe sample cross section photos is shown above (Fig. 16.)
Single GaN QFN 10x12mm samples using heat slug bonding passed MSL3 3x reflow test and 1,000 temperature cycle test (from -55°C to 125°C) and Power cycle test (121°C/100%RH, 192 hrs) without having any delamination failures and reliability test result is shown in below table 8.

Table 8. QFN10x12 with heat slug bonding reliability test result.

<table>
<thead>
<tr>
<th>TEST DESCRIPTION</th>
<th>SAMPLE SIZE</th>
<th>RESULT</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSL3 260°C 3X REFLOW</td>
<td>90</td>
<td>PASS (0/90)</td>
</tr>
<tr>
<td>TEMPERATURE CYCLE (-55°C/125°C)/1000 CYCLES</td>
<td>45</td>
<td>PASS (0/45)</td>
</tr>
<tr>
<td>PCT (121°C/100%RH) 192HRS</td>
<td>45</td>
<td>PASS (0/45)</td>
</tr>
</tbody>
</table>

Fig. 17. PCT 192hrs with MSL3 precondition

After PCT 192hrs completed, there is no delamination on samples as shown above Fig. 17.

Fig. 18. Temp cycle 1000 cycles with MSL3 precondition

After 1,000 temperature cycle completed, there is no delamination on samples are observed as shown above Fig. 18.

Fig. 19. Cross section after Temp cycle 1000 cycles

VIII. Further improvement of thermal performance and MSL level improvement

Cross section photos of post temperature cycle have been taken to check delamination inside the package (Fig. 19). After 1,000 temperature cycle completed, micro delaminations are observed on the edge of heat slug bonding fillet area which shows Ag sintering attach and heat slug adhesion degraded after temperature cycle, and no micro delamination is observed under GaN die attach region. Further study will be conducted to improve adhesion between heat slug and Ag sintering fillet area to achieve better MSL level and extended temperature cycles.

VIII. Conclusions

In this paper, QFN-SIP thermal improvement solutions are suggested for integrated driver and GaN mosfet in 8x8mm QFN-SIP package and per simulation the major thermal improvement comes from increasing body size and GaN die location and thickness of leadframe and Ag sintering attach and Cu clip bonding as descending order.

References