By LEE SMITH
Vice President, Advanced Packaging Products

11 Myths About SiP

By Lee Smith, UTAC Group

1. There is industry agreement on what a system in package (SiP) is.

   Not even close. The definition of SiP varies so widely, that the first chapter of TechSearch International's recent SiP report (1) includes a list of over 20 definitions of SiP from a range of SiP suppliers and users. To establish the basis for the report and forecasts, the chapter provides the following definition:
   "System-in-Package is a functional system or subsystem assembled into a standard footprint package such as LGA, FBGA, QFN, or FO-WLP. It contains two or more dissimilar die, typically combined with other components such as passives, filters, MEMS, sensors, and/or antennas. The components are mounted together on a substrate to create a customized, highly integrated product for a given application. SiPs may utilize a combination of advanced packaging including bare die (wire bond or flip chip), wafer level packages, pre-packaged ICs such as CSPs, stacked packages, stacked die, or any combination of these."

   Multichip packages (MCP) and multichip modules (MCM) are not considered a SiP in this definition but may be represented as SiP by various suppliers. This increases the challenge of analyzing and forecasting the SiP market. Many MCPs are combinations of devices like in stacked die chip scale packages (CSP) where flash and RAM are combined in a die stack supplied in high volumes. Or with MCM or modules where the solution is a custom assembly format that is not a standard package platform like a fine pitch ball grid array (FBGA).

2. SiP competes with SoC.

   They are more complimentary than competitive. System on a chip (SoC), has long been a very effective strategy to integrate

Originally published in Electronic Design

established IP blocks for high volume applications that can absorb the significant CMOS design and mask costs (which can exceed $300M) associated with a SoC (2). However, today's system and semiconductor designers are looking for heterogenous integration solutions like SiP that:

- Have faster time to market.
- Lower design, NRE and development costs (rarely exceed $100k).
- Can integrate semiconductor devices (active and passive) that do not scale well in CMOS.

3. SiP requires KGD.

   KGD is not required but may be necessary. Many SiP products are assembled with die that rely on the same wafer probe test coverage as used in a single chip package. Known good die (KGD) may be the right quality and reliability strategy for a complex SiP that requires a costly substrate or component bill of materials (BOM). For high volume SiP assembly, die are supplied in wafer form, so defining the best probe flow (which could include burn-in or voltage screening) is critical in developing your KGD strategy and supply chain. (3)

4. Heterogeneous integration (HI) will replace SiP.

   HI should be viewed as the broad big picture view for semiconductor technology road mapping beyond Moore's Law. Whereas SiP is the integration of various semiconductor devices within a given package platform. The International Technology Roadmap for Semiconductors (ITRS) is transitioning from a concentration of roadmaps for semiconductor fabrication scaling to outline the roadmap challenges and requirements for heterogeneous integration technologies. (4)

5. SiP requires a PCB laminate substrate.

Due to strong demand for passive integration (primarily capacitors and inductors) in power management applications, leadframe based SiPs are seeing strong growth. Prismark Partners forecasts the over 5 billion leadframe based power modules would ship by 2020 (5). Leadframes provide low cost and high thermal conductivity making them a strong SiP platform for lower I/O, higher power requirements. Laminate based SiPs in land grid array (LGA) and ball grid array (BGA) configurations, primarily assembled in strip formats, serve the widest range of SiP applications. Laminates support higher density interconnection requirements with wide design flexibility due to the wide range of laminate fabrication technologies. Wirebond, flip chip (FC), stacked die, embedded die or passives, and high density SMT are all readily enabled through laminate substrates.

Emerging high wiring density applications are shrinking conductor line and space widths below 12 microns with roadmaps below 5 microns. This is driving adoption and development of new SiP platforms such as FanOut wafer or panel level CSP or the use of silicon or glass based interposers with high aspect ratio thru vias.

6. SiP is a planar 2D assembly.

   With the growth in die stacking, package in package assembly, package on package (PoP) stacking and embedded die technologies, 3D package architectures are providing size and performance advantages over 2D planar assemblies. 3D SiP solutions can provide the following performance advantages:

   - 3D SiP can not only provide package footprint reduction on a printed circuit board assembly (PCBA), but enables an increase in semiconductor content to package ratio thru 3D integration technologies. Increased semiconductor content includes 3D integration of both active and passive devices.
   - Reductions in package footprint can provide improvements in package warpage control, associated improvements in PCBA assembly as well as improvements in second level solder joint reliability.

- Can provide improved electrical performance thru short vertical interconnects that can reduce circuit delays.
- Can enable EMI / RFI shield isolation between semiconductor devices for RF and digital integration requirements.

7. The SiP architecture, process technologies and materials are more critical than the supply chain business model.

   The supply chain business model can make or break success of a SiP in the market. A SiP solution can have 100 components in the electronic bill of materials (eBOM) but if 1 component is not available due to delivery or quality problems, SiP manufacturing is stalled.

   SiP solutions required advanced microelectronic package assembly and test capabilities. With the strong trend to outsource manufacturing services in the semiconductor and electronics industry over the past 50 years, outsourced semiconductor assembly and test (OSAT) providers have been the leaders in developing and scale up of advanced packaging technologies. The OSAT business model as a contract package assembly test provider to their semiconductor customers has been based on consignment of wafers. So OSAT supply chains have focused on equipment, circuit carriers (leadframe, substrate etc…) and materials requirements. The growth in SiP has been driven by smartphone applications over the past 15 years which has required OSAT supply chains to develop sources for electronic components. However, OSATs procure a very small percent of electronic components (estimated than 1%), so in a constrained business environment for electronic components, which we are currently in (escalating component prices and lead times) demanding a full turnkey business model could adversely impact a SiPs cost and time to market. Thus, SiP customers should team with OSAT suppliers in defining the optimum business model.

   - Consignment model – where SiP customer procures and consigns the eBOM, which the OSAT provider manages.
   - Pass through pricing (PTP) model – where SiP customer has contractual agreements for key components and establishes

supply terms for pass through pricing for the OSAT to procure at the contractual terms.
    - This is very common when custom components are specified or the customer has a limited source of components qualified.
- Full turnkey model – where the SiP customer requires the OSAT provider to source and manage the eBOM.
- Combination business model – where certain key components may be consigned or managed as PTP and standard components need to be procured by the OSAT or contract manufacturer.

8. There are no new business models in the semiconductor industry.

   With the record number and value of mergers and acquisitions in the semiconductor industry the past 3 years (6), industry analysts and trade editors focused on the trends and consequences of strong market consolidation. With the high cost of entry into the slowing and highly competitive semiconductor industry analysts speculated that the industry is nearly closed to new entries and new business models. Speculating that the following business models will continue to dominate the industry going forward:

   - IDM (integrated device manufacturer) - who owns and maintains semiconductor fabrication factories.
   - Fabless device suppliers - with focus on design, IP and rely on contract manufacturers to fabricate, assemble and test their devices.
   - Foundry suppliers – who provides contract semiconductor fabrication services to Fabless and IDM suppliers.

However, SiP technology is enabling a new semiconductor industry business model to emerge. That of an electronic systems integration provider that relies on advanced substrate and microelectronic assembly technologies to design a system or subsystem solutions by integrating various semiconductor devices, delivered in a SiP format. Octavo Systems is an example of this emerging business model (7). Figure 1, illustrates the semiconductors (bare and packaged ICs) used in Octavo's

OSD335x-SM product delivered in a 21 x 21mm 256 ball BGA SiP solution.

Octavo Systems website is a good source of information on the trends and solutions available through SiP as a systems integration platform. To understand the potential this new business model of a systems integration solution provider can achieve, explore the product innovations and new services emerging for internet of things (IoT) applications. New IoT applications are emerging across all industries including; banking, manufacturing, retail, health care, transportation, utilities and government. The revenue potential for IoT based products and services is forecasted to approach $270 billion by 2020 (8).

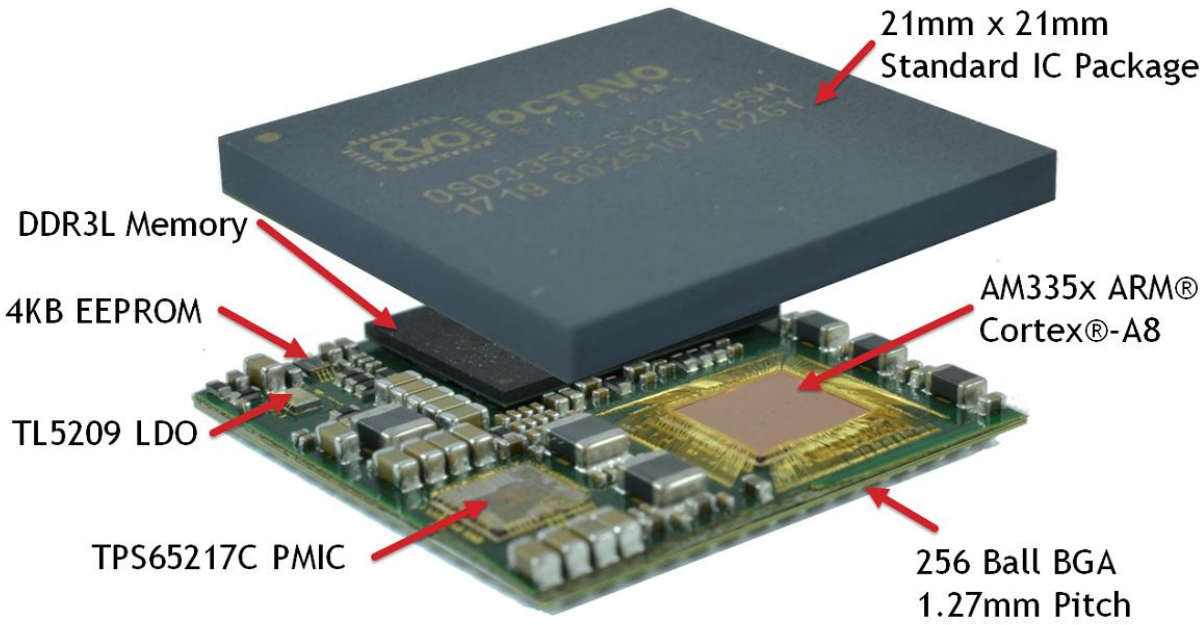

Figure 1. Octavo Systems OSD335x-SM BGA SiP based product.

9. SiP is only used for miniaturization.

Miniaturization is a key advantage of SiP but performance and system optimization are equally important in today's thrust for higher levels of integration. Many OEM system suppliers have added engineers with

strong microelectronic packaging experience to help them better define system architectures and new supply chains to expand their use of SiP and module solutions. They have support from electrical, thermal and mechanical design / simulation teams that have the tools needed for system performance or reliability optimization. Semiconductor and OSAT suppliers have also expanded their engineering and design / simulation teams to apply a broader range of advanced packaging technologies to develop new SiP solutions. Semiconductor foundries and electronic manufacturing service (EMS) providers have also added skills and capabilities to provide highly integrated solutions like SiP or modules. The use of SiP is quickly expanding in lower performance applications like IoT connectivity and high-performance systems like 5G networks.

10. SiP is limited to a sole source supply chain.

Not true. Multi-sourcing is a common requirement for high volume applications. A wide range of OSATs have advanced package assembly capabilities and offer broad SiP services. If multi-sourcing is required for your high volume or assurance of supply requirements; it is recommended to develop supply chain strategies to address:

- Copy exact or copy equivalent requirements. Copy equivalent allows for suppliers to apply their qualified material sets as well as enabling alternate sources for passive components.
- Multi-source qualification.
- Market share agreements for sharing of volumes and maintaining capable sources of supply.
- Open sharing of design or manufacturing cost and quality improvements.
- End of life product management.

11. SiP is only economical for low performance applications.

SiP solutions are in production across a diverse range of applications. Computing, gaming, communications and networking require high

performance for challenging electrical, thermal and mechanical requirements with long product lives. SiP solutions are not only not limited to low performance requirements but along with 3D SiP architectures can enable miniaturization and semiconductor integration to enhance system performance through increasing bandwidth, lowering power, enabling increased functionality and integration of mixed semiconductor process nodes; in smaller product footprints with increased time to market.

References:

(1) "SiP for Mobile and Wearable Applications, Market Forecasts and the Changing Business Model"; TechSearch International Multiclient Report, Feb. 2016

(2) "How Much Will That Chip Cost?", March 27, 2014, Ed Sperling http://semiengineering.com/how-much-will-that-chip-cost

(3) "Known Good Die: A Closer Look, Test Methods and Reliability Screens," Solid State Technology, Larry Gilg http://electroiq.com/blog/2005/02/known-good-die-a-closer-look

(4) "ITRS 2.0: Toward a re-framing of the Semiconductor Technology Roadmap" https://ieeexplore.ieee.org/abstract/document/6974673/

(5) Prismark Partners

(6) IC Insights website, News and Bulletins http://www.icinsights.com/news/bulletins/Value-Of-Semiconductor-Industry-MA-Deals-Slows-Dramatically-In-2017

(7) Octavo Systems website, Products https://octavosystems.com/octavo_products/osd335x-sm

(8)"Internet of Things Market to Reach $267B by 2020," https://www.forbes.com/sites/louiscolumbus/2017/01/29/internet-of-things-market-to-reach-267b-by-2020/#25959f2b609b

(9) Intel FBGA and SoC products https://www.altera.com/products/sip/overview.html